Power Supply Access Impedance Boost to Improve PLC Systems Performance

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Abstract: This paper highlights the critical need to address the access impedance in power supplies used in power line communication (PLC) modems. Low values of access impedance of power supplies can significantly attenuate PLC signals at both the transmitter and receiver nodes, leading to substantial degradation in performance. To mitigate this issue, we propose a modified boost power factor correction circuit capable of enhancing the access impedance magnitude of power supplies in PLC modems across a frequency band ranging from 0 to 500 kHz. Numerical analyses show the effectiveness of our proposal in comparison to other existing circuits. Furthermore, these results suggest promising directions for further enhancements in the performance of PLC systems.

Keywords: power line communication, transmitter, receiver, signal degradation, power supply.

1. INTRODUCTION

In the leading edge of modern connectivity lies power line communication (PLC), a technology that leverages existing electric power grids for data communication purposes (Ribeiro et al., 2024). Within the spectrum of PLC, the utilization of ultra narrowband (UNB) and narrowband (NB) frequency bands, covering the frequencies between 0 and 500 kHz, is relevant for several electric utility applications (Galli et al., 2011). UNB and NB frequency bands exhibit exceptional propagation properties, enabling communication over short and long distances, as well as in both urban and rural areas (Galli et al., 2011; Malik et al., 2018). An advantage of utilizing UNB and NB frequency bands is the effortless transmission through distribution transformers (Rieken et al., 2014) and capacitor banks, giving the freedom to use low-cost coupling at the low-voltage levels (da Silva Costa et al., 2022), and low transmission power with minimal risk of causing interference to other components on the electric power grid (Hunt and Hunt, 1995).

It is well-established that the propagation of PLC signals through electric power grids is challenging due to the dynamics of loads, characteristics of power cables, topologies of electric power grids, the use of unshielded power cables, and the proliferation of electronics-based loads and renewable energy sources, among other things (da S. Costa et al., 2019). Overall, these elements collectively contribute to composing the electric power grid access impedance (González-Ramos et al., 2023). Ongoing investigations into the electric power grid impedance, exemplified by recent studies (da S. Costa et al., 2019), highlight its non-stationary and random behavior. Specifically, research within the Brazilian low voltage (LV) network indicates significant variations in the electric power grid impedance attributed to diverse loads and topologies. In other words, connecting PLC modems to the electric power grid is not a simple task (De Piante and Tonello, 2016).

Current PLC technologies are well-advanced to overcome several problems related to connecting PLC modems to the electric power grid. However, a not-yet-addressed and particular problem refers to the wasted power of the transmitted and received PLC signals with the power supply of PLC modems. If the power supply of PLC modems is not properly designed, then fractions of PLC signals are wasted at the transmitter and receiver sides, resulting in additional signal degradation.

In this paper, we pay attention to the access impedance of power supplies of PLC modems in UNB and NB frequency bands (i.e., frequencies between 0 and 500 kHz). In this sense, we provide a simplified model from which we can easily identify the degradation on PLC signals associated with power supplies of PLC modems. In the sequel, we introduce a modified boost power factor correc-

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tion (PFC) circuit to increase the magnitude of the access impedance of power supplies used by PLC modems that can reduce this degradation. Numerical results show the improvements attained with the proposal compared to the boost PFC circuit and the rectifier circuit with an electromagnetic compatibility (EMC) filter. Moreover, these results point out an interesting direction for additional improvements to PLC systems.

2. PROBLEM FORMULATION

Figure 1 illustrates a block diagram of a PLC modem connected to the electric power grid. This PLC modem is supposed to operate in the frequency band between 0 and 500 kHz, covering UNB and NB frequency bands. A short description of each block is as follows:

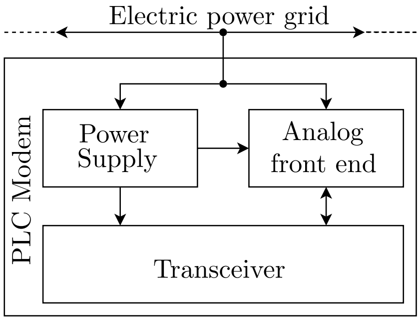

Figure 1. PLC modem block diagram.

- **Power Supply**. It supplies energy to the main blocks of the PLC modem (i.e., analog front end and transceiver). Due to its compactness, efficiency, and electrical isolation, it usually features a switching topology, such as the flyback converter.
- **Analog front end**. It provides signal conditioning and safe electric coupling between the transceiver and the electric power grid. It encompasses a power amplifier, automatic gain control, digital-to-analog and analog-to-digital converters, and a coupling circuit.
- **Transceiver**. It is responsible for generating carrying-information waveforms transmitted through the PLC channel and ensuring the transmitted information is reliably recovered from the waveforms, which are supposed to be distorted by interference and additive noise, at the receiver side.

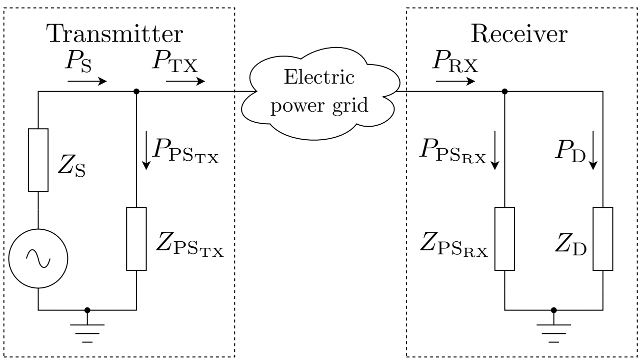

Figure 2. A simplified model of the unidirectional communication between two PLC modems.

Now, let us consider a unidirectional data communication between two PLC modems, i.e., from the transmitter to the receiver, as depicted in Figure 2. The signals transmitted by the PLC modem are modeled as zero-mean stationary random processes. They are impaired by additive noise modeled as a zero-mean stationary and colored Gaussian random process. Also, we assume that the coupling circuit is an ideal passband analog filter.

Based on these assumptions, a simplified model can be derived to characterize the power flow from the transmitter to the receiver, as in Figure 2. In this simplified model, the transmitter front end is modeled as a voltage source in series to an impedance Z_{S}. The power delivered by this source to transmit the information through the electric power circuit is denoted by P_{S}. For the frequency band occupied by the PLC signal, the power supply of the transmitter is modeled as an impedance $Z_{\mathrm{PS_{TX}}}$ and, consequently, it consumes the power $P_{\mathrm{PS_{TX}}}$. In other words, part of P_{S}, which is used to transmit information through the electric power grid, is consumed by the transmitter power supply. At the receiver side, the power supply is modeled as $Z_{\mathrm{PS_{RX}}}$ and consumes the power $P_{\mathrm{PS_{RX}}}$. Also, the receiver front end is modeled as an impedance Z_{D}.

Therefore, the effective transmitted power is

$$P_{\mathrm{TX}} = P_{\mathrm{S}} - P_{\mathrm{PS_{TX}}} \,. \tag{1}$$

Consequently, the received power at the input of the receiver is given by

$$\begin{aligned} P_{\mathrm{RX}} &= P_{\mathrm{TX}} \|h(t)\|_2^2 + P_{\mathrm{V}} \\ &= \left(P_{\mathrm{S}} - P_{\mathrm{PS_{TX}}}\right) \|h(t)\|_2^2 + P_{\mathrm{V}}, \end{aligned} \tag{2}$$

where $\|\cdot\|_2$ is the Euclidean norm and $h(t) \in \mathbb{R}, -\infty < t < +\infty$, is the impulsive response of the electric circuit between transmitter and receiver, and P_{V} is the additive noise power. Due to the presence of the power supply at the receiver, the power at the input of the front end is given by

$$\begin{aligned} P_{\mathrm{D}} &= P_{\mathrm{RX}} - P_{\mathrm{PS_{RX}}} \\ &= \left(P_{\mathrm{S}} - P_{\mathrm{PS_{TX}}}\right) \|h(t)\|_2^2 + P_{\mathrm{V}} - P_{\mathrm{PS_{RX}}} \\ &= P_{\mathrm{S}} \|h(t)\|_2^2 - \left(P_{\mathrm{PS_{TX}}} \|h(t)\|_2^2 + P_{\mathrm{PS_{RX}}}\right) + P_{\mathrm{V}}, \end{aligned} \tag{3}$$

where $P_{\mathrm{PS_{RX}}}$ is the fraction of the received power consumed by the receiver's power supply. Note that a fraction of the received power P_{RX} is consumed by the receiver's power supply, which is also modeled as the impedance $Z_{\mathrm{PS_{RX}}}$ in the frequency band occupied by the PLC signal. Consequently, only the power P_{D} is delivered to the analog front end.

From (3), we note that the term $P_{\mathrm{PS_{TX}}}$ and $P_{\mathrm{PS_{RX}}}$ can severely reduce the power P_{D} if the power supplies at both transmitter and receiver sides are not well-designed. Moreover, the terms $\|h(t)\|_2^2$ and P_{V} cannot be controlled since they refer to the degradation suffered by the PLC signal when transmitted through the electric power grid and the noise corruption, respectively. Based on the provided assumptions, the signal-to-noise ratio (SNR) at the input of the receiver front end is given by

$$\gamma = \frac{P_{\mathrm{D}} - P_{\mathrm{V}}}{P_{\mathrm{V}}} = \frac{P_{\mathrm{S}}\|h(t)\|_2^2 - \left(P_{\mathrm{PS_{TX}}}\|h(t)\|_2^2 + P_{\mathrm{PS_{RX}}}\right)}{P_{\mathrm{V}}}. \quad (4)$$

In (4), P_{S}, $P_{\mathrm{PS_{TX}}}$, and $P_{\mathrm{PS_{RX}}}$ can be adjusted. Considering that $P_{\mathrm{S}} \leq P_{\max}$, we come up with the conclusion that the maximization of γ can only be attained with the minimization of both $P_{\mathrm{PS_{TX}}}$ and $P_{\mathrm{PS_{RX}}}$ since $\|h(t)\|_2^2$ and P_{V} cannot be controlled. To the best of the authors' knowledge, PLC modem designs do not take into account the problem caused by $Z_{\mathrm{PS_{TX}}}$ and $Z_{\mathrm{PS_{RX}}}$. Consequently, they do not include constraints in order to minimize $P_{\mathrm{PS_{TX}}}$ and $P_{\mathrm{PS_{RX}}}$. However, the provided formulation based on a simplified model theoretically shows a remarkable problem if power supplies are designed with no regard to the presence of PLC signals. According to the formulation, the design of PLC modem power supplies must offer the highest possible impedance for all frequencies except for the mains frequency f_{o}, for which it has the impedance Z_{nom}, compatible with its nominal power. Ideally, the PLC modem power supply should have the following input impedance:

$$Z_{\mathrm{PS}_l}(f) = \begin{cases} Z_{\mathrm{nom}} & , \text{if } f = f_{\mathrm{o}} \\ \infty & , \text{otherwise} \end{cases} \quad (5)$$

in which $l \in \{\mathrm{TX}, \mathrm{RX}\}$.

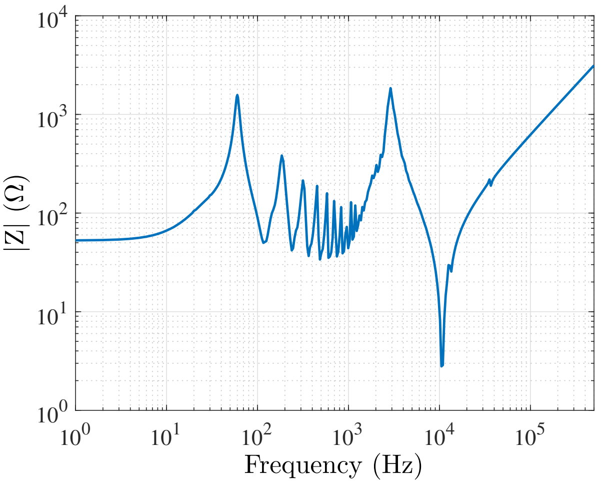

Figure 3. Access impedance of a typical rectifier with an EMC filter.

An illustration of the reported problem is presented in Figure 3. This figure shows the access impedance of a typical rectifier with an EMC filter, similar to the one detailed in (STMicroelectronics, 2016) and designed for NB PLC modems. Note that in the frequency band occupied by PLC signals (i.e., $0 - 500$ kHz), the power supply access impedance is low compared to the characteristic impedance of LV cables (Kharraz et al., 2016), resulting in considerable values of $P_{\mathrm{PS_{TX}}}$ and $P_{\mathrm{PS_{RX}}}$. This is not convenient for a PLC modems since part of the transmitted/received power will be wasted in the power supply rather than being used for data communication.

In the field of power electronics, there are concerns about the presence of harmonics and low power factors. High total harmonic distortion (THD) and low power factor degrade the performance of equipment connected to the electric power grid. A circuit commonly used to address these concerns is the active PFC circuit (Figueiredo et al., 2010). It replaces the power supply rectifier, using a switching converter topology (such as the boost converter) and control circuitry to achieve a high power factor, regardless of the nature of the load. Consequently, it reduces the injection of harmonics into the electric power grid (De Gussemé et al., 2007). However, boost PFC circuits are not designed to reject UNB and NB PLC signals. Nonetheless, with a few modifications, they can also be harnessed for rejecting these signals. In this sense, Section 3 details a modified version of the boost PFC to accomplish it.

3. THE MODIFIED BOOST PFC CIRCUIT

In this section, we detail a modified version of the boost PFC circuit that can improve the power supply performance by increasing its access impedance in UNB and NB frequency bands. Figure 4 illustrates the block diagram of the modified boost PFC circuit with an analog controller. In this block diagram, Z_{T} is the impedance of the power line between the mains voltage source and the modified boost PFC circuit, A_1 and A_2 denote isolated amplifiers responsible for normalizing voltage amplitudes, Z_{M} represents the circuitry of a PLC modem fed by the power supply, and V_{ref} denotes the reference voltage for feeding the PLC modem circuitry. Moreover, D refers to a diode, and C and L represent a capacitor and an inductor, respectively.

The voltage signal $v(t)$ at the input of the modified boost PFC circuit is constituted by the mains signal (e.g., 50 Hz or 60 Hz), the PLC signal, and the additive noise (e.g., harmonics, supra harmonics, etc.). According to Fig. 4, the modified boost PFC circuit differentiates from the conventional one by the introduction of a bandpass analog filter, centered at f_{o}, to yield at its output $v_{\mathrm{o}}(t)$ only the mains voltage signal, which is a sinusoidal waveform. Therefore, other components of $v(t)$ are considered distortions. By dealing with these distortions, the modified boost PFC circuit not only achieves a high power factor but also creates a high power supply access impedance in UNB and NB frequency bands.

Note that the modified boost PFC circuit operates by cyclically switching the MOSFET Q, controlling the current flow through the inductor L. As the goal is to achieve high impedance in UNB and NB frequency bands by controlling the input current, the switching frequency of MOSFET Q must be at least twice the upper frequency of the desired converter bandwidth (Sheehan and Anatole, 2007). Although a switching frequency above 1 MHz is feasible, there is a trade-off regarding switching losses and component selection.

Moreover, the analog controller contains an inner current loop, responsible for controlling the current through the inductor, and an outer voltage loop, responsible for the output voltage control. For the current loop to be effective, its proportional-integral (PI) compensator must be tuned

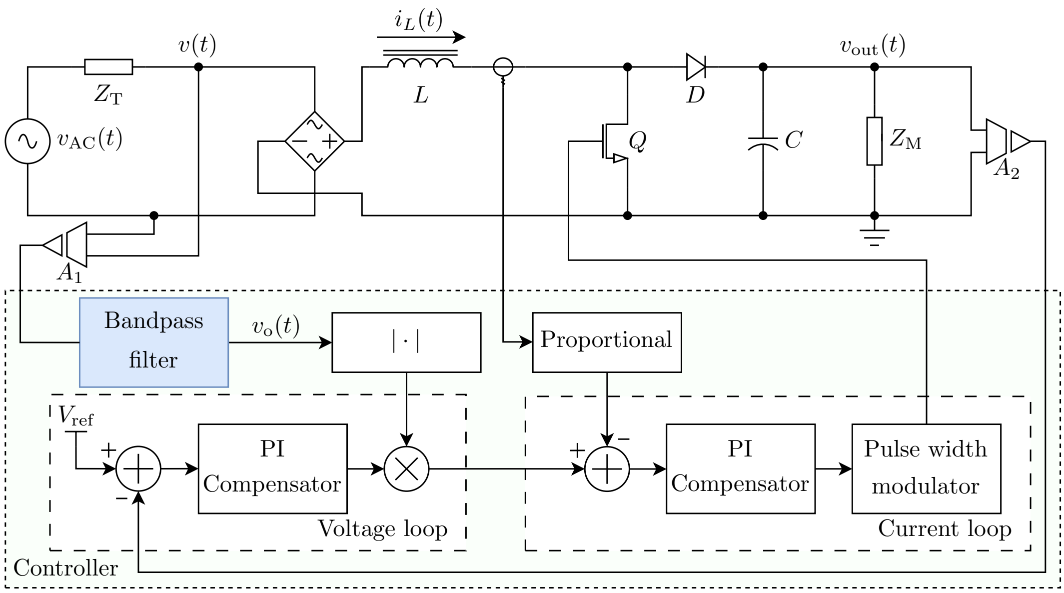

Figure 4. The modified boost PFC circuit with analog controller.

so that the current closed-loop transfer function has the desired bandwidth (in our case, $0-500$ kHz) with a phase margin that ensures stability.

Note that a digital version can replace the analog controller. In this case, PI compensators, proportional and absolute value operators, and bandpass analog filter are substituted for their digital counterparts. The digital controller also includes zero-order hold blocks for sampling the continuous-time signals and a unitary delay block before the pulse width modulator.

4. NUMERICAL RESULTS

To analyze the improvement attained with the modified boost PFC circuit, simulations were carried out on PSIM® when both analog and digital controllers were used. The simulation results refer to the PLC modem operating as a transmitter since similar results are attained when the PLC modem operates as a receiver.

In the analog controller, a fourth-order elliptic analog filter was chosen to perform the bandpass filtering (Schaumann et al., 2001). Figure 5 shows its magnitude and phase responses. Note that zero-phase and almost unitary gain is attained at 60 Hz, meaning that the boost PFC circuit will have access to a good estimate of the mains voltage signal. The design of a fourth-order elliptic digital filter can be easily obtained, as detailed in (Mitra, 2006).

To facilitate the numerical analysis, the modified boost PFC circuit with an analog controller is compared with the conventional boost PFC circuit and the rectifier circuit with an EMC filter. The parameter used for comparison is the access impedance of each circuit in UNB and NB frequency bands.

The block diagram of the simulation setup used to emulate the PLC signal transmission and carry out numerical simulations is shown in Figure 6. Note that the voltage source $v_{AC}(t)$ is modeled by an ideal sinusoidal waveform of 127 V root mean square and 60 Hz. The impedance of the power line $Z_T = 0.8 + j2\pi 40 f\mu\ \Omega$ was experimentally

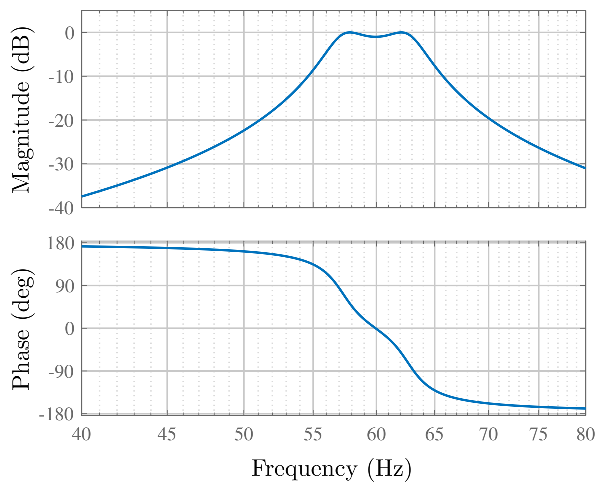

Figure 5. Designed fourth-order elliptic bandpass analog filter.

obtained with a 50 meter multistrand 2.5 mm^2 PVC-insulated copper power cable. A current source of 100 mA ($i_S(t)$) was used to generate a sinusoidal with a frequency ranging from 0 to 500 kHz. For each frequency value obtained with a resolution of 1 Hz, the amplitudes of $v(t)$ and $i_{PS_{TX}}(t)$ for the chosen frequency were collected for each circuit in the device under test (DUT) (i.e., the modified boost PFC circuit, the conventional boost PFC circuit, and the rectifier with an EMC filter). Dividing the amplitude of voltage and current for each chosen frequency allows us to emulate the division of $|V(f)| = |\mathcal{F}\{v(t)\}|$ by $|I_{PS_{TX}}(f)| = |\mathcal{F}\{i_{PS_{TX}}(t)\}|$ and, consequently, estimate the access impedance at the DUT, i.e., $Z_{PS_{TX}}(f)$. Note that $\mathcal{F}\{\cdot\}$ and $|\cdot|$ denote the continuous-time Fourier transform and absolute value operator, respectively.

All circuits were configured to consume a nominal power of 10 W, and the boost PFC circuits to have an output voltage of $v_{out}(t) = 200$ V. Table 1 lists the values of components used to design the conventional and modified

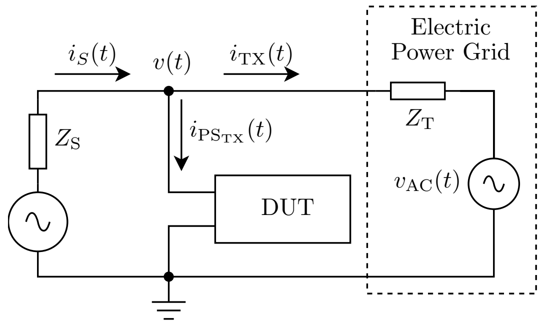

Figure 6. Simulation setup to carry out performance analyses.

PFC circuits. The rectifier with EMC filter based on (STMicroelectronics, 2016) includes a 3165 Ω resistor as a load for a power consumption of 10 W.

Table 1. Component values of both conventional boost PFC and modified boost PFC circuits.

Component	Value
L	5 mH
C	6 μF
Z_M	4 kΩ

4.1 Analog controller

Figure 7 shows the magnitude of the access impedance for the modified boost PFC circuit with analog controller, the conventional boost PFC circuit with analog controller, and the rectifier with an EMC filter. Note that the modified boost PFC circuit offers the highest access impedance, followed by the conventional boost PFC, which offers a relatively flat response across the spectrum. This is consistent with the principle that a power factor-corrected circuit resembles a resistor. The lowest access impedance is attained by the rectifier with an EMC filter.

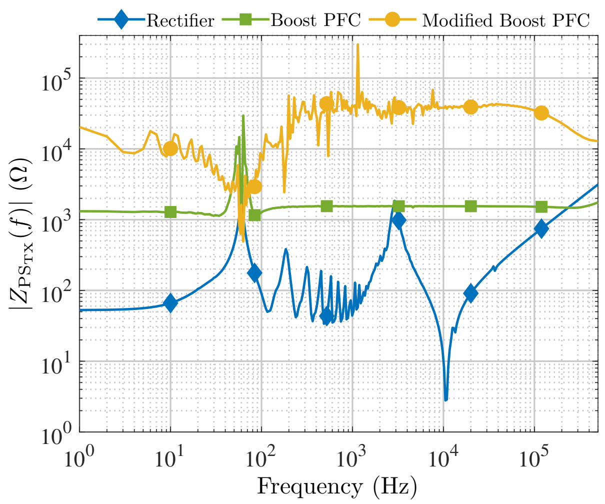

Figure 7. Simulation results when analog controller is considered.

4.2 Digital controller

Next, we analyze the magnitude of the access impedance when a digital controller is applied to both modified boost PFC and conventional boost PFC circuits, as shown in Figure 8. Again, the attained results show that the modified boost PFC circuit offers the highest values and is closely followed by the conventional boost PFC circuit for frequencies below 10 kHz. Moreover, we observe lower impedance values for the modified boost PFC circuit starting from 8 kHz compared to those obtained with the analog controller. This is an expected behavior, as the digital controller requires a more limited bandwidth to maintain stability. In fact, for frequencies above 10 kHz, the access impedance of both modified boost PFC and conventional boost PFC circuits become very similar, different from what happened in the analog version of the circuits.

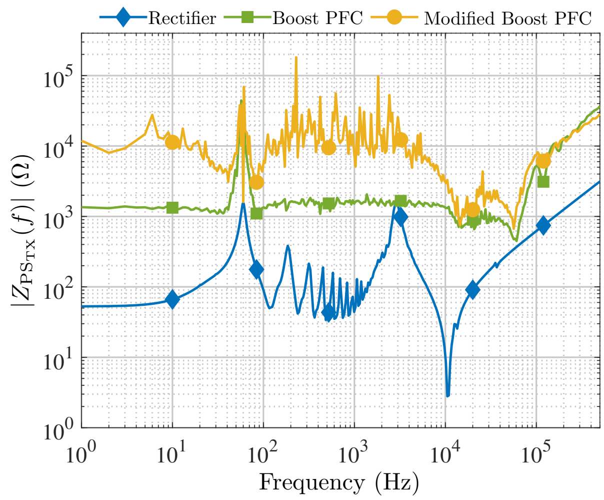

Figure 8. Simulation results when digital controller is considered.

5. CONCLUSIONS

In this paper, we have addressed the necessity of increasing the magnitude of access impedance of power supplies used by PLC modems. This simple yet critical assessment avoids wasting part of transmitted and received PLC signals power. Aiming to deal with this problem, we have also proposed a small modification to the boost PFC circuit to increase the magnitude of its access impedance in UNB and NB frequency bands. A performance comparison between the modified boost PFC circuit, the conventional boost PFC circuit, and the rectifier circuit with an EMC filter was carried out. The numerical results showed that the modified boost PFC circuit can effectively increase the magnitude of the access impedance of power supplies used in PLC modems. Future works aim to investigate other improvements in the digital controller and build a prototype to carry out field tests.

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