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Analysis and Design of Isolated SEPIC Converter with Greinacher Voltage Multiplier Cell

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Abstract: High step-up converters are required and used in photovoltaic applications, due to low voltage of photovoltaic modules. In this paper, an isolated dc-dc high step-up SEPIC with a Greinacher voltage doubler cell is presented. It has the advantage of continuous input current, high efficiency, high voltage gain, isolation and demands a single switch, being suitable for low power grid-tie photovoltaic systems. The operating principles and steady-state analysis are presented, including the detailed analysis of resonant stage, where the value of primary side capacitor is taken into account and plays an important role in the design of the converter, since it directly affects the resonance frequency and RMS current values. Simulation results are presented to validate the analysis and design.

Keywords: Isolated SEPIC, Resonant stage, Voltage multiplier cell.

1. INTRODUCTION

The increase of photovoltaic systems, specifically low power grid-tie systems with two converters, makes high-step up dc-dc converter very important. These systems, as shown in Fig. 1, are also known as AC photovoltaic modules (module-integrated-converter – MIC), where a high step-up converter, in first stage, provides a high voltage gain and is connected to a grid-tie inverter. Galvanic isolation is desirable to maintain security of the whole system, besides mitigating leakage current and electromagnetic interference (EMI) problems (Kjaer et al. 2005).

Single-switch converters are more suitable for lower power applications, reducing volume, costs and complexity. Basic single-switch isolated topologies are: flyback, ZETA, SEPIC and Ćuk. Among these options, isolated SEPIC converter is a very good choice, since it provides continuous input current and can significantly reduce the dc magnetizing current with the appropriate choice of voltage multiplier cells (VMCs), allowing to use a transformer instead of coupled inductor (Williams. 2016).

VMCs applied on secondary side provide the advantages of increased converter static gain and clamped voltage spikes on diodes without elevating voltage stress over the switch, unlike

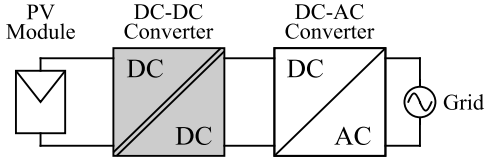

Fig 1 MIC converter with emphasis on first stage.

VMCs applied on primary side. These VMCs used on secondary side are based on switched-capacitor techniques and the most commonly used are known as voltage doubler (VD) and voltage tripler (VT), with the possibility of expansion to raise voltage gain, although increasing the number of converter components (Forouzesh et al. 2017).

The goal of this work, besides showing operating principles, is to deduce the main equations of the selected converter, proving the accuracy of these equations, obtained considering the value of primary side capacitor, instead of Kim et al. (2015), where this element is disregarded, resulting in a contribution that has not been reported yet. Section 2 briefly shows the reasons to choose the converter topology. In section 3, theoretical analysis is made, including principle of operations and equations of all stages, besides the equations of current and voltage ripples, rms and the static gain of converter. Simulation results are presented in section 4, showing converter operation and the accuracy of the equations, comparing theoretical and simulation results. Finally, in section 5, some relevant conclusions about the work are made.

2. DERIVATION OF CONVERTER

The isolated SEPIC converter, shown in Fig. 2b is obtained from the classic topology, shown in Fig. 2a. Cantilever model can be used to represent the magnetic element (transformer or coupled inductor) (Erickson et al. 1998). Fig. 2c shows the converter with VMC on secondary side. Greinacher VD cell, Dickson and Ladder VT cells, shown in Fig. 3, can be used on secondary side. As mentioned before, an appropriate choice of VMC can significantly reduce the dc magnetizing current, guaranteeing that the magnetizing inductance, L_m, does not store energy. Thus, a transformer is used for galvanic isolation instead of a

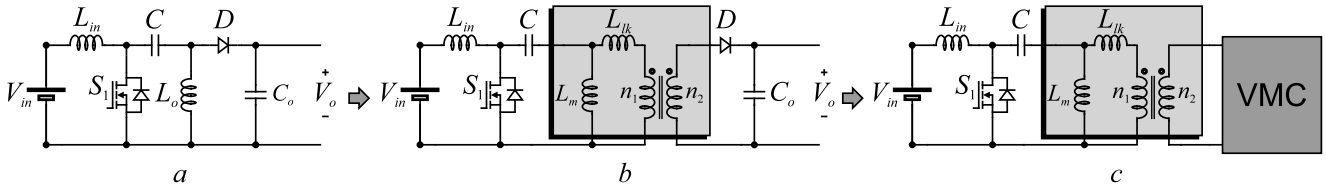

Fig 2 Isolated SEPIC derivation: (a) Classic SEPIC converter; (b) Isolated SEPIC using cantilever model; (c) Isolated SEPIC with VMC on secondary side.

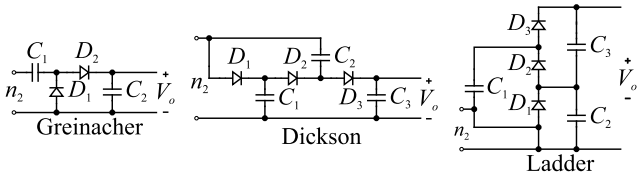

Fig 3 Voltage multiplier cells used on secondary.

coupled inductor, consequently providing a better utilization of BxH curve, reducing its volume and its leakage inductance, L_{lk} (Witulski. 1995). This can be achieved by the use of VD, but it is not possible with VT cells. Table I summarizes the voltage gain of cells and the static gain of converters obtained with the insertion of these VMCs, based on (Alzahrani et al. 2019), (Axelrod et al. 2008) and (Yao et al. 2015), where D is duty cycle of converter and n is the transformer turn ratio.

Table 1. Voltage and static gain of cells and converters.

Cell	Voltage gain	Topology	Static Gain (M)
–	–	SEPIC	$D/(1-D)$
–	–	Isolated SEPIC (iSEPIC)	n$D/(1-D)$
Greinacher	$1/D$	VDiSEPIC	n/(1-D)
Dickson and Ladder	$(1+D)/D$	VTiSEPIC	n(1+D)/(1-D)

3. THEORETICAL ANALYSIS OF THE CONVERTER

The circuit of isolated SEPIC with VD Greinacher cell (VDiSEPIC) is shown in Fig. 4. In order to evaluate the theoretical performance of this converter, the following features are approached in this section: principle of operation, voltage gain derivation, voltage stress and current stress.

3.1 Principle of operation

In order to simplify the steady-state analysis, the following assumptions are made:

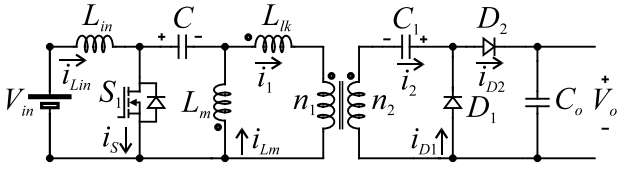

Fig 4 Topology circuit of VDiSEPIC.

1) All power devices are ideal;
2) The magnetizing inductor, L_m, is taken into account on the analysis, however, using a transformer with high quality material and good design, its impact is irrelevant, once its inductance is much higher than leakage inductance, L_{lk};
3) Output voltage is constant, therefore, capacitor C_o is not taken into account on the analysis.

Fig. 5 shows the key waveforms of the converter in one switching period, T_s, in continuous-conduction-mode (CCM). It is important to mention that these waveforms are obtained for operation below resonance frequency. This can be better understood with Fig. 6, where the three operations modes are presented. The best option is the first mode, nearly to second mode, where total switching losses are smaller. This will receive more attention during the description of operation stage 2, where this resonance occurs. The converter has four operation stages in one switching period, as shown in Fig. 7. The converter operation is given as follows:

Stage I ($t_0 - t_1$): This stage begins when switch S_1 is turned on, and the primary current i_1 begins its linear decreasing, as well as current i_2, while switch current, i_S, slowly increases also linearly. This results in a quasi-ZCS turn on of the switch. This stage ends when current i_1 reaches 0 A and diode D_2 is turned off under ZCS condition. The duration of this stage is considerably smaller than stage II and, because of this, voltages across capacitors are constant on this stage. The main equations of this stage are given by

$$v_{C1}(t) = nV_{in} - \frac{\Delta v_{C1}}{2} = v_{C1\_\min} \tag{1}$$

$$v_C(t) = V_{in} + \frac{\Delta v_c}{2} = v_{C\_\max} \tag{2}$$

$$i_{Lin}(t) = i_{Lin}(t_0) + \frac{V_{in}}{L_{in}}t, \tag{3}$$

$$i_1(t) = ni_2(t) = ni_{D2} = i_1(t_0) + \frac{-v_{C\_\max} + \frac{v_{C1\_\min} - V_o}{n}}{L_{lk}}t, \tag{4}$$

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{v_{C\_\max}}{L_m}t, \tag{5}$$

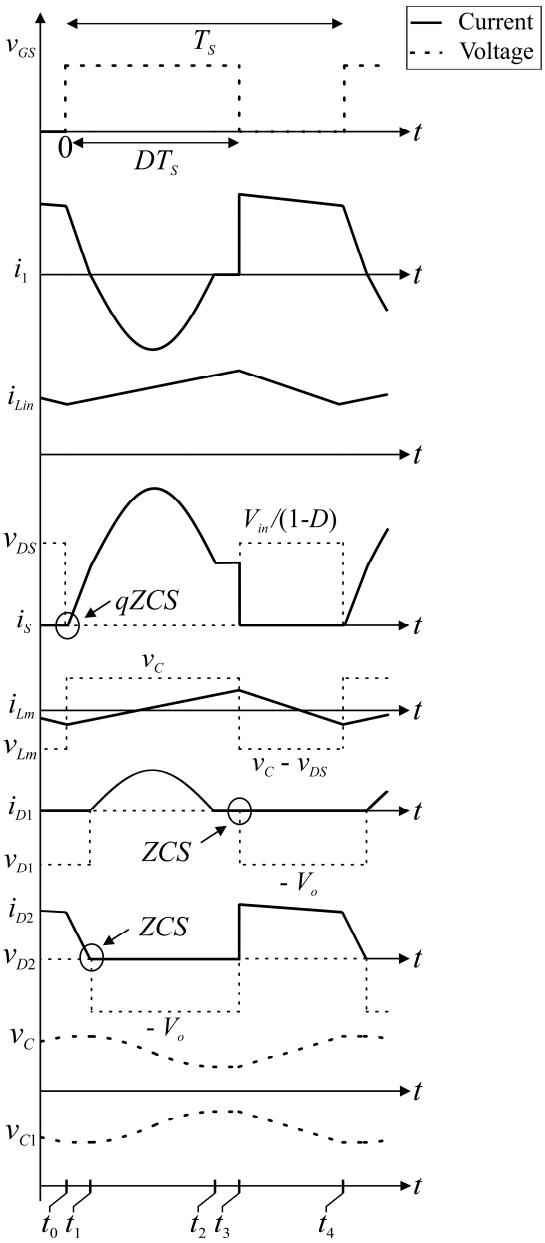

Fig 5 Key waveforms of VDiSEPIC in CCM operation.

$$i_s(t) = i_{Lin}(t) + i_{Lm}(t) - i_1(t). \tag{6}$$

Stage II (t_1 – t_2): This stage begins when current i_1 changes its direction, so diode D_1 is turned on. At this instant, a resonance occurs among C, L_{lk} and C_1, hence currents and voltages are sinusoidal, charging the capacitor C and discharging C_1. Voltage across L_{in} still being equal to V_{in}, and voltage across L_m is equal to v_C, so, both currents are increasing linearly. To analyse this resonance, it is necessary to obtain the equivalent circuit for this stage, shown in Fig. 8.

Magnetizing inductance is significantly higher than leakage inductance, and its ac ripple current is reduced, so, this element can be neglected in resonance analysis. In Fig. 8, inductance L_{lk} is referred to secondary multiplying its inductance by square of turn ratio, n^2, and C is referred to secondary as C_S, dividing its capacitance by n^2. The equivalent capacitance is composed by a

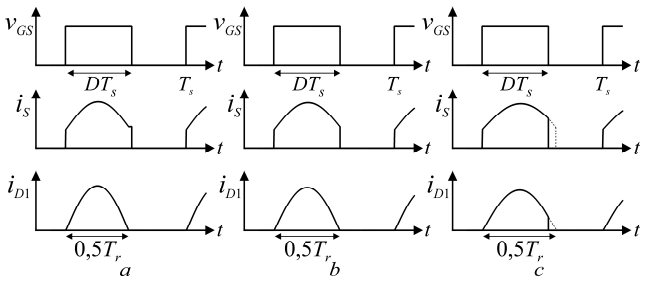

Fig 6 Converter operation according to variation of resonance: (a) below resonance operation – first mode: $DT_s > 0.5T_r$; (b) exactly resonance operation – second mode: $DT_s = 0.5T_r$; (c) above resonance operation – third mode: $DT_s < 0.5T_r$.

series association of C_s and C_1. Therefore, C_{eq}, resonance frequency, f_r, and resonant impedance, Z_r, are given by

$$C_{eq} = \frac{C_1 \dfrac{C}{n^2}}{C_1 + \dfrac{C}{n^2}}, \tag{7}$$

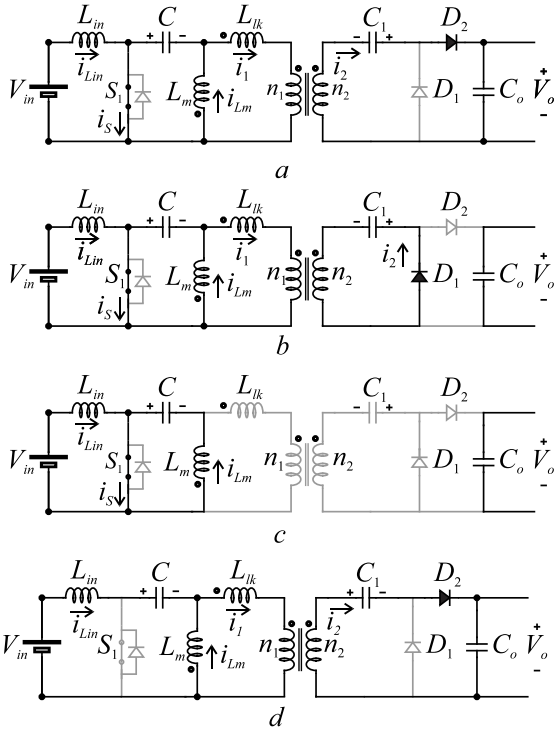

Fig 7 Current flow path in four stages during one switching period in CCM operation: (a) stage I; (b) stage II; (c) stage III; (d) stage IV.

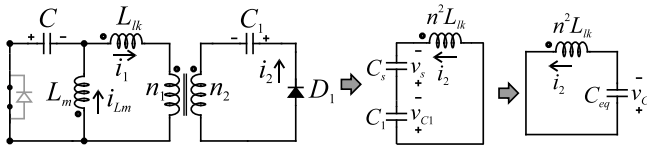

Fig 8 Converter equivalent circuit of resonant stage.

$$f_r = \frac{1}{2\pi\omega r}; \frac{1}{T_r} = \frac{1}{2\pi\sqrt{C_{eq} n^2 L_{lk}}}; \; Z_r = \sqrt{\frac{n^2 L_{lk}}{C_{eq}}}. \quad (8)$$

Hence, as mentioned before, there are three possibilities of operation regarding to resonance frequency, switching period and duty cycle. The best choice are values of T_r, T_s and D that make converter operate in first mode, near to second mode. In this case, ZCS condition is guaranteed to D_1, besides root mean square (RMS) and peak value of i_s and i_{D1} are the smallest possible.

To solve the circuit, it is necessary to use Kirchhoff's voltage law (KVL), obtaining

$$v_{n^2 Llk} - v_{Ceq} = 0 \rightarrow +n^2 L_{lk} \frac{di_2}{dt} - \frac{1}{C_{eq}} \int_{t_1}^{t_2} i_{Ceq} dt + v_{Ceq}(0) = 0. \quad (9)$$

Considering that $i_{Ceq} = -i_2 = -i_1/n$, and applying Laplace Transform over (9), yields

$$+sn^2 L_{lk} \frac{i_1}{n}(s) - n^2 L_{lk} \frac{i_1}{n}(0) + \frac{i_1(s)}{nsC_{eq}} - \frac{v_{Ceq}(0)}{s} = 0, \quad (10)$$

where $i_1(0)$ and $v_{Ceq}(0)$ are the initial conditions of current and voltage, respectively. Rearranging terms, current i_1 can be obtained, given by

$$i_1(s) = \frac{n\left(C_{eq}(+sn^2 L_{lk} i_1(0) + v_{Ceq}(0))\right)}{s^2 n^2 L_{lk} C_{eq} + 1}. \quad (11)$$

Considering $i_1(0) = 0$ A, once its value is null at begin of stage 2, and applying inverse Laplace Transform, i_1 is obtained in time domain, given by

$$i_1(t) = ni_2(t) = -ni_{D1} = n\sqrt{\frac{C_{eq}}{n^2 L_{lk}}} v_{Ceq}(0)\sin(w_r t), \quad (12)$$

where $v_{Ceq}(0)$ is obtained by the difference between $v_{C1}(0)$ and $nv_C(0)$. Finally, considering that $i_C = i_1$, and $i_{C1} = -i_1/n$, and applying the equation of capacitor voltage in s domain, the main equations are given by

$$\begin{aligned} v_C(t) &= \frac{Cv_C(0) + C_{eq} n v_{Ceq}(0) + \left(-C_{eq} n v_{Ceq}(0))\cos(w_r t)\right)}{C} \\ v_{C1}(t) &= \frac{C_1 v_{C1}(0) - C_{eq} v_{Ceq}(0) + \left(C_{eq} v_{Ceq}(0)\cos(w_r t)\right)}{C_1} \end{aligned} \quad (13)$$

$$i_{Lin}(t) = i_{Lin}(t_1) + \frac{V_{in}}{L_{in}} t, \quad (14)$$

$$i_{Lm}(t) = i_{Lm}(t_1) + \frac{v_C(t)}{L_m} t, \quad (15)$$

$$i_s(t) = i_{Lin}(t) + i_{Lm}(t) - i_1(t) \quad (16)$$

This stage ends when current i_1 reaches 0 A, and, consequently, diode D_1 is turned off under ZCS condition.

Stage III ($t_2 - t_3$): This stage begins when switch is still on, but there is no current left on transformer and diodes are off, so, voltage v_{C1} is constant, equal to the value at the end of stage II. Once the duration of this stage is considerable smaller than previous stage, and C is in series with L_m, its voltage, v_C, also can be considered constant. This stage ends when S_1 is turned off, with losses, without soft-switching. Similar to stage 1, this stage is very small and it happens in first and second modes of operation, but not in third. The main equations are given by

$$v_{C1}(t) = nV_{in} + \frac{\Delta v_{C1}}{2} = v_{C1\_\max}, \quad (17)$$

$$v_C(t) = V_{in} - \frac{\Delta v_c}{2} = v_{C\_\min}, \quad (18)$$

$$i_{Lin}(t) = i_{Lin}(t_2) + \frac{V_{in}}{L_{in}}\left(t - \frac{T_R}{2}\right) = i_{Lin\_\max}, \quad (19)$$

$$i_{Lm}(t) = i_{Lm}(t_2) + \frac{v_{C\_min}}{L_m}\left(t - \frac{T_R}{2}\right) = i_{Lm\_\max}, \quad (20)$$

$$i_s(t) = i_{Lin}(t) + i_{Lm}(t). \quad (21)$$

Stage IV ($t_3 - t_4$): This stage begins when switch is turned off and diode D_2 is turned on, and there is current flux on transformer. Differently from stage 2, this one occurs without resonance, and, consequently, currents and voltages are not sinusoidal, charging capacitor C and discharging C_1. During this stage, the voltage across L_{in} is the difference between V_{in} and V_{DS}, resulting in a linear decreasing of i_{Lin}, while voltage across L_m is the difference between v_C and V_{DS}, also resulting in a linear decreasing of i_{Lm}. This stage ends when switch is turned on. The main equations are given by

$$v_C(t) = v_{C\_\min} + \frac{1}{C}\begin{pmatrix} i_{Lin\_\max}(t - DT) - \ldots \\ -\frac{(t - DT)^2 (V_{DS} - V_{in})}{2L_{in}} \end{pmatrix} \quad (22)$$

$$v_{C1}(t) = v_{C1\_\max} - \frac{1}{nC_1}\begin{pmatrix} i_{Lin\_\max}(t - DT) + .. \\ +i_{Lm\_\max}(t - DT) - .. \\ -\frac{(t - DT)^2 (V_{DS} - V_{in})}{2L_{in}} - .. \\ -\frac{(t - DT)^2 (V_{DS} - V_{in})}{2L_m} \end{pmatrix} \quad (23)$$

$$i_{Lin}(t) = i_{Lin\_\max} - \frac{(V_{DS} - V_{in})}{L_{in}}(t - DT), \quad (24)$$

$$i_{Lm}(t) = i_{Lm\_\max} - \frac{(V_{DS} - V_{in})}{L_m}(t - DT), \quad (25)$$

$$i_1(t) = i_{Lin} + i_{Lm} = ni_2(t) = ni_{D2}. \quad (26)$$

3.2 Voltage Gain Derivation

To obtain the static gain of this converter, it is necessary to apply the volt-second balance to the input inductor, L_{in}, during the four operation stages, given by

$$\frac{1}{T_s}\left(\int_{t_0}^{t_1} v_{Lin}dt + \int_{t_1}^{t_2} v_{Lin}dt + \int_{t_2}^{t_3} v_{Lin}dt + \int_{t_3}^{t_4} v_{Lin}dt\right) = 0. \quad (27)$$

Considering that stages I and III are much smaller than stages II and IV, it is possible to neglect them. So, (27) can be rewritten as

$$\frac{1}{T_s}\left(\int_{0}^{DT} v_{Lin}dt + \int_{DT}^{T} v_{Lin}dt\right) = 0. \quad (28)$$

Voltages across L_{in} on stages II and IV are, respectively, V_{in} and V_{in} - V_{DS}. So, substituting these variables in (28) and solving the integrals, it is obtained

$$\left(DV_{in} + (1-D)(V_{in} - V_{DS})\right) = 0. \quad (29)$$

From analysis of stage IV, it is possible to affirm that the $V_{in} - V_{DS}$ can be substituted by $-V_o/n + V_{in}$. So, substituting this in (29) and rearranging the terms, static gain is obtained and it is given by

$$M = \frac{V_o}{V_{in}} = \frac{n}{1-D}. \quad (30)$$

3.3 Voltage and Current Stress

The voltage stress over the switch is given by

$$V_{DS} = \frac{V_{in}}{1-D}. \quad (31)$$

For diodes D_1 and D_2, the voltage stresses are given by

$$V_{D1} = V_{D2} = -V_o. \quad (32)$$

It can be seen that even with the increase in static gain, voltage stress on switch is the same of classical isolated SEPIC, while voltage stress on diodes is smaller.

As to RMS current values on diodes, it can be used the theory of general piecewise waveform, where a periodic waveform, composed of N piecewise segments has a RMS value of

$$RMS = \sqrt{\sum_{k=1}^{N} D_k u_k}, \quad (33)$$

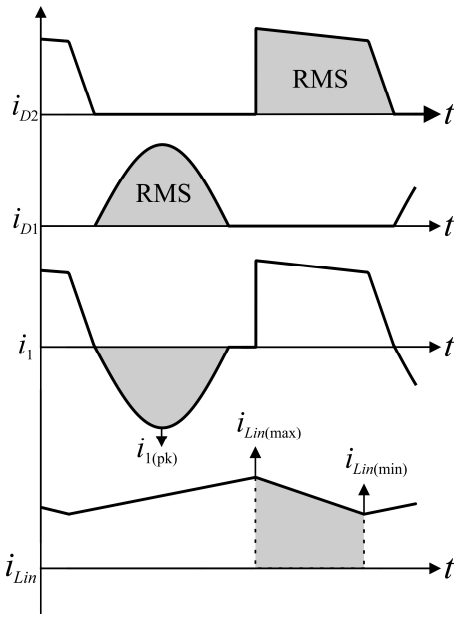

Fig 9 Key waveforms to calculate RMS of i_{D1} and i_{D2}.

where D_k is the duty cycle of segment k, and u_k is the contribution of segment k. The contribution depends on the shape of the segment. To better understand this, in Fig. 9 some waveforms and crucial points to calculate RMS of i_{D1} and i_{D2} are shown.

According to (Erickson et al. 2001), current i_{D2} has a trapezoidal segment, while i_{D1} has a sinusoidal segment. From analysis of operation stages, it can be affirmed that i_{D1} is equal to i_1 referred to secondary in stage II. In the same way, i_{D2} is equal to i_{Lin} referred to secondary in stage IV. The portion of i_{D2} during the stage I is neglected, since the duration of this stage is considerably smaller than the duration of stage IV and, therefore, it does not affect the RMS current evaluation. D_k of segment u_k of i_{D1} is equal to $0.5T_r/T_s$, resulting in a RMS equation given by

$$i_{D1(rms)} = \frac{i_{1(rms)}}{n} = \frac{\sqrt{\frac{1}{2} i^2_{1(pk)} \frac{0.5T_r}{T_s}}}{n}. \quad (34)$$

D_k of segment u_k of i_{D2} is equal to (1-D), resulting in a RMS equation given by

$$i_{D2(rms)} = \frac{\sqrt{u_{iLin}(1-D)}}{n};$$
$$i_{D2(rms)} = \frac{\sqrt{\frac{1}{3}\left(i^2_{Lin(\min)} + i_{Lin(\min)} i_{Lin(\max)} + .. + i^2_{Lin(\max)}\right)(1-D)}}{n}. \quad (35)$$

Finally, as to switch RMS value, it is necessary to use the classical equation of RMS variable, once i_s waveform does not have a defined equation, given by

$$i_{s(rms)} = \sqrt{\frac{1}{T_s}\int_0^{T_s} {i_s}^2 dt} = \sqrt{\frac{1}{T_s}\left(\begin{array}{l}\left(\int_0^{T_r/2}\left(-i_1 + i_{Lin}\right)^2 dt\right) + .. \\ + \left(\int_{T_r/2}^{DT_s} {i_{Lin}}^2 dt\right)\end{array}\right)}. \quad (36)$$

Substituting i_1 and i_{Lin} by its equations previously presented in (36), results in

$$i_{s(rms)} = \sqrt{\frac{1}{T_s}\left(\begin{array}{l}\int_0^{T_r/2}\left(\begin{array}{l}-\sqrt{\frac{C_{eq}}{n^2 L_R}}(v_{Ceq}(0))sin(w_r t)n + .. \\ + i_{Lin\_\min} + \frac{V_{in}}{L_{in}}t\end{array}\right)^2 dt + .. \\ + \int_{T_r/2}^{DT_s}\left(i_{Lin\_\min} + \frac{V_{in}}{L_{in}}t\right)^2 dt\end{array}\right)}. \quad (37)$$

The solution of this equation will give

$$i_{s(rms)} = \sqrt{\frac{1}{T_s}\left(a - \frac{\left(\frac{b+c}{3}\right)}{{L_{in}}^2} + d + e - f - \left(\frac{g+h}{L_{in}}\right)\right)}, \quad (38)$$

where

$$k = \left(\left(\frac{1}{2f_r}\right) - DT_s\right), \quad (39)$$

$$a = \left(\frac{1}{2f_r}\right){i_{Lin\_\min}}^2 - {i_{Lin\_\min}}^2 k, \quad (40)$$

$$b = {V_{in}}^2\left(kD^2{T_s}^2 + DT_s\left(\frac{1}{2f_r}\right) + \left(\frac{1}{2f_r}\right)^2\right), \quad (41)$$

$$c = L_{in}\left(3V_{in}i_{Lin\_\min}\left(\frac{1}{2f_r} + DT_s\right)\right)k \quad (42)$$

$$d = \frac{\left(\frac{1}{2f_r}\right)^3 {V_{in}}^2}{3{L_{in}}^2} + \frac{\left(\frac{1}{2f_r}\right)^2 V_{in}i_{Lin\_\min}}{L_{in}} + 6C_{eq}v_{Ceq(0)}i_{Lin\_\min}, \quad (43)$$

$$e = \frac{C_{eq}\left(\frac{1}{2f_r}\right){vc_{eq(0)}}^2 3^2}{2n^2 L_{lk}} - 6C_{eq}v_{Ceq}(0)i_{Lin\_min}\cos\left(wr\frac{1}{2f_r}\right), \quad (44)$$

$$f = \frac{{C_{eq}}^{3/2}v_{Ceq}(0)^2 3^2\cos\left(wr\frac{1}{2f_r}\right)\sin\left(wr\frac{1}{2f_r}\right)}{2\sqrt{n^2 L_{lk}}}, \quad (45)$$

$$g = 6C_{eq}\left(\frac{1}{2f_r}\right)v_{Ceq}(0)V_{in}\cos\left(wr\frac{1}{2f_r}\right), \quad (46)$$

$$h = 6{C_{eq}}^{3/2}\sqrt{n^2 L_{lk}}v_{Ceq}(0)V_{in}\sin\left(wr\frac{1}{2f_r}\right). \quad (47)$$

3.4 Voltage and current ripples

The voltage and current ripples are obtained by the integral of current on inductor and voltage of capacitor in a switching period, analyzing and rearranging the therms. So, current ripple of i_{Lin} is given by

$$\Delta i_{Lin} = i_{Lin}(DT) - i_{Lin}(0) = \frac{1}{L_{in}}V_{in}DT. \quad (48)$$

Voltage ripple of v_C is given by

$$\Delta v_c = v_c(T) - v_c(DT) = \frac{I_{in}(1-D)}{Cf_s}. \quad (49)$$

Voltage ripple of v_{C1} is given by

$$\Delta v_{c1} = v_{c1}(DT) - v_{c1}(T) == \frac{I_{in}(1-D)}{nC_1 f_s}. \quad (50)$$

4. SIMULATION RESULTS

This section presents simulation results of the VDiSEPIC converter, in order to verify the theoretical analysis approached in this paper. The simulation was performed with the parameters presented in Tab. 2, using a time step of 0.2 ns.

Table 2. Parameters of simulation.

Parameter	Value
Output power	200 W
f_s	24 kHz
T_s	16.66 µs
V_{in}	37.4 V
V_o	404.3 V
D	0.445
n	1:6
L_{in}	1 mH
L_{lk}	1 µH
L_m	1 mH
C	33 µF
C_1	9.155 µF
C_o	100 µF
R	821.13 Ω

Input voltage was chosen from the optimum operating voltage under Standard Test Conditions of PV module CS5A-200, from Canadian Solar, which has a nominal maximum power of 200 W. Duty cycle and turn ratio were defined so that the output voltage is around 400 V, keeping duty cycle at a maximum value of 0.5 and turn ratio at a maximum value of 6.

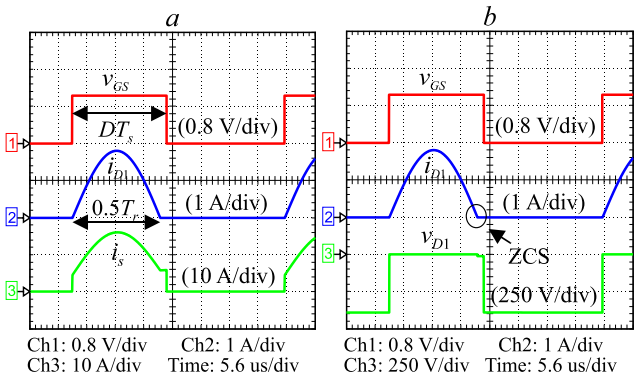

Fig 10 (a) Simulated waveforms of v_{GS}, i_s and i_{D1}; (b) Simulated waveforms of v_{GS}, i_{D1} and v_{D1}.

Input inductor, L_{in}, was chosen for a maximum current ripple of 15%, while primary capacitor, C, and resonant capacitor C_1, were chosen for a maximum voltage ripple of 10% and 1%, respectively. As the transformer was not designed, leakage inductor was chosen to guarantee converter operation in first mode, near to second mode. Magnetizing inductor was chosen with an inductance thousand times higher than leakage inductance. Finally, load resistor, R, was chosen in order that output power is 200 W.

Using (8), the calculated resonance frequency is equal to 29.059 kHz, while in simulation it is equal to 29.036 kHz, resulting in a small difference of 23 Hz, less than 1% of error. v_{GS}, i_s and i_{D1} are shown in Fig. 10*a*. As can be seen in this figure, converter is operating in first mode, near to second mode. Considering the values of duty cycle, and switching period, the total time that switch is ON is 18.542 µs, while half of resonant period is 17.21 µs. Once converter is operating in first mode, ZCS condition is obtained in D_1, as can be seen in Fig. 10*b*, where diode forward voltage is -403.1 V, equal to $-V_o$.

To verify the theoretical static gain of converter, using (30), the value obtained is 10.811, while in simulation it is equal to 10.78, once that V_o is practically constant, with 403.1 V and V_{in} is 37.4 V. Fig. 11*a* shows voltages of capacitors C and C_1. Fig 11*b* shows only ac component, to verify the ripple of v_C and v_{C1}. Δv_C simulated is 3.723 V, while Δv_{C1} simulated is 2.234 V. Using (49) and (50), calculated Δv_C is 3.73 V, while calculated Δv_{C1} is 2.241 V, resulting in a small error less than 1%.

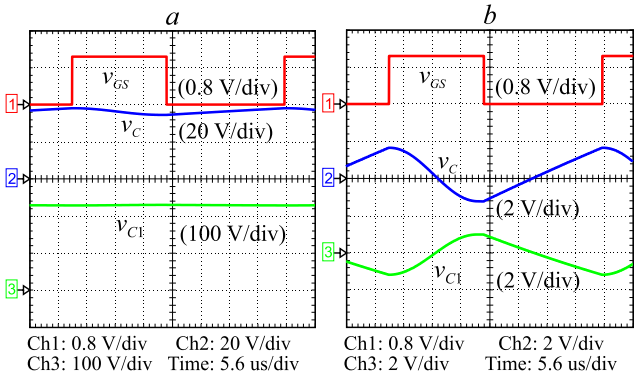

Fig 11 (a) Simulated waveforms of v_{GS}, v_C and v_{C1}; (b) ripple of v_C and v_{C1}.

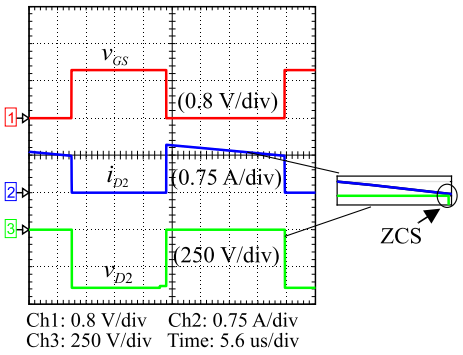

Fig 12 Simulated waveforms of v_{GS}, i_{D2} and v_{D2}.

Fig. 12 shows waveforms of v_{GS}, i_{D2} and V_{D2}, with zoom on turn-off instant of D_2. This zoom gives a better view of ZCS condition. Forward voltage of D_2 is equal to V_{D1}, -403.1 V.

Fig. 13 shows waveforms of v_{GS}, i_s and v_{DS}, with zoom on turn-on instant of S_1. This zoom gives a better view of quasi-ZCS condition. Voltage stress on the switch is 67.2 V, being in agreement with theoretical value using (31).

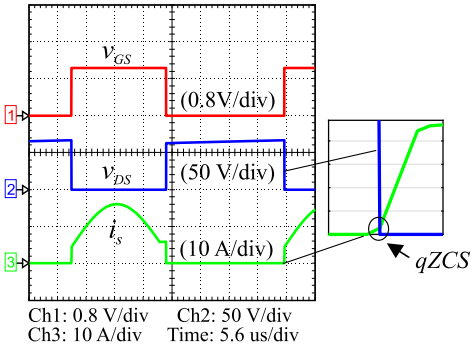

Fig 13 Simulated waveforms of v_{GS}, v_{DS} and i_s.

Finally, Fig. 14*a* shows waveforms of v_{GS}, i_{Lm}, i_1 and i_{Lin}. Fig. 14*b* shows only ac component of i_{Lin}, to verify the ripple of this current. Δi_{Lin} simulated is 0.692 A, while calculated Δi_{Lin}, using (48), is 0.693 A, also with an error less than 1%.

Table 3 shows a comparison of the simulated and calculated main parameters of the converter. These results show that all equations obtained in theoretical analysis have a good accuracy,

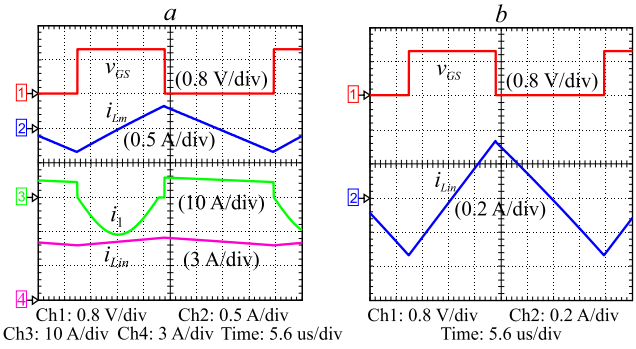

Fig 14 (a) Simulated waveforms of v_{GS}, i_{Lm} and i_{D1}; (b) ripple of i_{Lin}.

with a small error, less than 1%, in comparison with simulated results.

Table 3. Comparison of calculated and simulated parameters.

Parameter	Calculated	Simulated	Error (%)
f_r (kHz)	29.059	29.036	23 (0.08)
M	10.81	10.78	0.03 (0.3)
$V_{D1} = V_{D2}$ (V)	-404.3	-403.1	1.2 (0.3)
V_{DS} (V)	67.388	67.2	0.188 (0.28)
i_{D1} (rms) (A)	0.855	0.848	0.007 (0.82)
i_{D2} (rms) (A)	0.664	0.66	0.0044 (0.67)
i_s (rms) (A)	8.406	8.334	0.072 (0.85)
Δi_{Lin} (A)	0.693	0.692	0.001 (0.14)
Δv_C (V)	3.73	3.723	0.007 (0.188)
Δv_{C1} (V)	2.241	2.234	0.006 (0.3)

5. CONCLUSIONS

This work presented a dc-dc high step-up SEPIC with a Greinacher VD cell, used as primary stage of a MIC converter. Its derivation was made, showing that VD cell is an appropriate choice. Theoretical analysis was made, showing operating principle of all stages, besides obtaining the equations used for comparison with simulation results, including the resonant analysis considering primary capacitor.

Simulations results were performed and compared with theoretical values obtained from the equations. These results show a high static gain, without using a high turn ratio and high duty cycle. Besides that, all theoretical calculated values show a good accuracy in comparison with simulated results, proving that the analysis are correct.

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