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Single-Stage LED Driver with Dimming and Universal Input Voltage Capability

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Abstract: This paper presents a boost bridgeless totem-pole converter operating as power factor correction (PFC) stage integrated with a half-bridge LLC resonant converter as power control (PC) stage. The resultant single-stage converter yields in an effective integration, reducing the number of switches from 4 to 2 (50% reduction). This integrated topology aims decreasing conduction and commutation power losses and, moreover, achieving high power factor (PF), low total harmonic distortion (THD) and higher efficiency when compared with other converter structures. The converter is designed to have a fixed bus voltage, which is controlled by changing the half-bridge duty cycle under universal input voltage (UIV). However, since the HB duty cycle also affects the LLC converter due to their integration, a variable inductor is employed to control the LLC impedance and achieve a controlled output current and dimming capability. Simulation and experimental results are presented to verify the theorical analysis, through a 100 W LED luminaire. The results show voltage and current levels in the topology for different operating points. Moreover, it is shown the feasibility of output current control capability through variable inductor even with HB duty cycle variation.

Keywords: *LED driver, boost bridgeless converter, half-bridge LLC resonant converter, integrated topology, universal input voltage, dimming.*

I. INTRODUCTION

Given the increasing concerns about environmental and energy saving issues, light-emitting diodes (LEDs) are becoming the most used artificial lighting system in the world, being a research focus in the new generation of light source. The LED has several advantages in comparison with another electrical lighting sources, as high efficiency, superior life span and great luminous efficiency [1]–[4].

Energy conversion stages are used to adapt and stabilize current levels, providing appropriate current for the LEDs without deteriorating the quality of the consumed energy. These conversion stages compose the so-called electronic drivers, or LED drivers. In order to match the characteristics of the driver and the LED, several studies have been developed to achieve greater efficiency conversion, reduced size and elevated lifespan in electronic drivers for LEDs.

Usually two-conversion-stages are employed in AC/DC electronic drivers for LED supplying: PFC and PC stages. While the PFC stage aims power factor regulation, complying with harmonic standards of the International Electrotechnical Commission (IEC) 61000-3-2, the PC stage has a main objective: regulating current levels for the LEDs [5].

Among several topologies for LED drivers, the integrated single-stage has drawn considerable attention due to their features as high efficiency and simplified control circuit [6], [7]. Integrated single-stages are conceived with PFC and PC stages sharing their power switches functions and control circuits. However, integrating converters cause a problem: losing degrees of freedom, what results in reduced controllability. In this way, special functionalities as UIV and dimming demand an efficient topology development, much times impaired due to the integration.

Several integrated converters have been recently proposed and investigated [8]–[17] for artificial lighting applications. In [8] a dual buck-boost PFC converter with coupled inductors operating in DCM is integrated with a half-bridge LLC dc-dc resonant converter, designed for street-lighting application. Employing a boost converter as PFC, [9] investigates its integration with a half-bridge LLC resonant converter, where a fixed input voltage and controlled output current is noticed. A interleaved boost converter with shared boost inductor is employed as PFC in [10], being integrated with the LLC resonant converter. A resonant controller is employed and it works controlling the switching frequency, changing output current levels to achieve dimming capability. Already in [11], [12] and [13], the PFC stage converters are integrated to the LLC, achieving output current control while operates with a single input voltage value.

Recently, the LLC filter has been substituted by the CLCL version in integrations with PFC, as shown [14] and [15]. These new integrated converters seek for an improvement of fundamental characteristics in integrated converters, as elevated efficiency and good current regulation, but without working with UIV and dimming. The LC converter in employed with another PFC converters, as in [16] and [17], without operating with special functionalities. In addition, [18] proposes an integration without employing resonant converters, where buck-boost and SEPIC converters supplies a LED module.

On the other hand, since resonant converters presents high efficiency, efforts are directed to enhance the performance of

the PFC stage which is integrated with the half-bridge. One of these efficient PFC converters proposed is the boost bridgeless totem-pole [16]. Differently of other converters, this topology does not rely on a diode bridge rectifier [19]. Both switches operate in a complementary form, working as diode rectifier in one half-wave cycle and as power switches in another half-wave cycle. This characteristic provides reduction of diodes number in the conventional boost AC/DC converter (from five to two) but increase the number of switches (from one to two). This converter is a great alternative concerning improvement of efficiency in power converters.

One of the most used topologies employed on PC stages is the LLC converter [20]. The soft-switching characteristics of the LLC resonant circuit allow decreasing switches power losses. This characteristic allied with the reduced switches number of the PFC stage will provide a great efficiency. Besides, integrating both converters may be a great opportunity of efficiency improvement and reducing size. However, in order to allow further functionalities to the system since the controllability is diminish with the integration, alternatives are proposed to achieve UIV and dimming.

In this way, this work presents a single-stage converter, integrating the boost bridgeless totem-pole PFC converter and an LLC resonant PC converter. The bus voltage is controlled changing the duty cycle in the PFC stage, while the output current is adapted changing the impedance value associated with the series inductance through a variable inductor [21].

This paper is organized as follows: Section II shows the proposed topology analysis, section III shows PFC and PC design, Section IV shows simulation and experimental results, and Section V shows the conclusion of this work.

II. Proposed Topology and Circuit Analysis

A. Employed Topologies

As mentioned in section I, the boost bridgeless totem-pole converter works as PFC stage achieving high PF, while reduces significantly the number of semiconductors in the circuit. It is derived from the boost PFC converter, widely used in PFC applications [9], as it is shown in Fig 1(a).

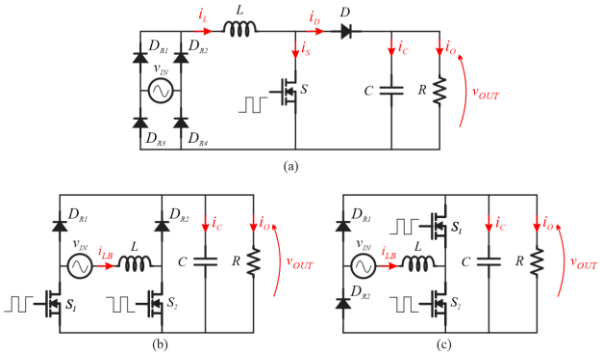


Fig. 1. (a) Boost PFC converter. (b) Boost bridgeless PFC converter. (c) Boost bridgeless totem-pole PFC converter.

Reallocating the switches of the boost PFC converter, it is possible to obtain the topology shown in Fig. 1(b), called boost bridgeless PFC. However, the connection of both switches in the ground of the load causes common-mode noise, raising the THD. To overcome this drawback, switches S_1 and the diode D_{R2} exchanges theirs positions on the circuit, creating the so-called boost bridgeless totem-pole PFC, shown in Fig. 1(c), which results in better efficiency than conventional boost topology [16] [22].

Fig. 2 shows the LLC resonant converter, a widely used converter in LED drivers due to its soft switching characteristics, as ZVS in primary side switches and ZCS in secondary side diodes [9]–[12].

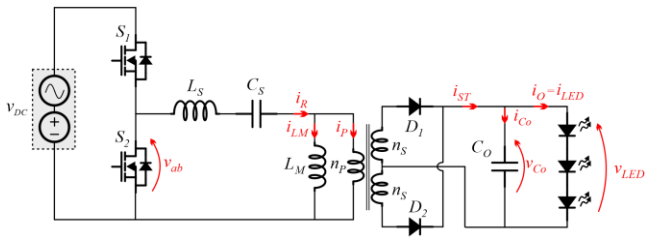


Fig. 2. LLC resonant converter.

The integration between the boost bridgeless totem-pole PFC converter and the LLC resonant converter is performed sharing their switches. The resulting single-stage converter is shown in Fig. 3. As it can be seen, the series inductor is composed by a variable inductor, which is responsible to control the output current. In addition, the half-bridge duty cycle is changed to maintain bus voltage controlled under load variation and UIV.

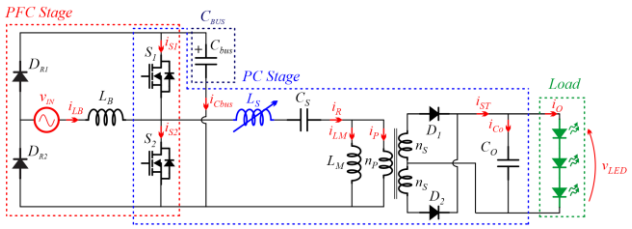


Fig. 3. Proposed integrated topology.

B. Operating Principle

After integrating the converters, it is necessary analyze its operation. The single-stage converter has a union of characteristics from PFC stage and PC stage. Operation stages are described as follows. All these operation stages consider steady-state operation.

Stage 1 (t_0 - t_1): Both switches S_1 and S_2 are off. The resonant current flows through the intrinsic diode of S_2. This current flowing through S_2 intrinsic diode, before S_2 turn-on, will make the terminal voltage in the switch be near of 0, achieving ZVS characteristic.

Stage 2 (t_1 - t_2): Assuming positive input semi-cycle, when S_2 turns on, V_{IN} charges the inductor L_B trough S_2 and D_{R2}. In this moment, while the resonant current falls, the current in L_B rises gradually. For now, the current direction in S_2 is not changed, changing when the current amplitude in L_B i_{LB} is higher than the current amplitude on the resonant circuit i_R, which characterize the end of this stage. During this step, the resulting amplitude current in S_2 is i_{S2}=i_{LB}-i_R.

Stage 3 (t_2 - t_3): With the resonant current i_R falling and the L_B current i_{LB} rising, this stage starts when the current amplitude in L_B turns higher than the resonant current. The current in L_B keeps increasing linearly and this stage ends when $i_R < 0$.

Stage 4 (t_3 - t_4): This stage begins when the direction of the resonant current changes. This makes the current in S_2 be

equals to the sum of the resonant current i_R and the current in L_B ($i_{S2}=i_{LB}+i_R$). This stage ends when switch S_2 turns off.

Stage 5 (t_4 - t_5): When S_2 turns off, the intrinsic diode of S_1 begins to be a path for current through the bus capacitor C_{bus}. The resonant current i_R begins flowing through it and the inductor L_B starts discharging, where $i_{S1}=i_{LB}+i_R$. This stage ends when S_1 turns on.

Stage 6 (t_5 - t_6): During this stage the switch S_1 is on. As occurred in stage 2, ZVS on the switch S_1 is achieved since intrinsic diode conducts before the switch is turning on. The inductor L_B keeps discharging and the current in S_1 is $i_{S1}=i_{LB}-i_R$. This stage ends when $i_R > 0$.

Stage 7 (t_6 - t_7): In this stage i_R becomes to be positive again. As i_{LB} keeps discharging normally and i_{S1} stills being $i_{LB}-i_R$. Analogously to stage 2 the current i_{LB} is decreasing while the current i_R is increasing. This stage ends when i_{LB} reaches in 0.

Stage 8 (t_7 - t_8): The inductor L_B is totally discharged. Consequently, the only current flowing through C_{bus} is the resonant current i_R, changing when S_1 turns off. The next stage will be the same as stage 1. The negative cycle is not shown in the analysis. However, the operation principle is the same as cited.

It is needed to make an emphasis about the charging and discharging of the output capacitor C_O. As will be seen later, the converter will operate with different operating points, through varying its duty cycle and series inductance. Thus, the order of some operation stages and the moment that capacitor C_O begins or finishes its charging or discharging may change. This question relies of the operating point analyzed.

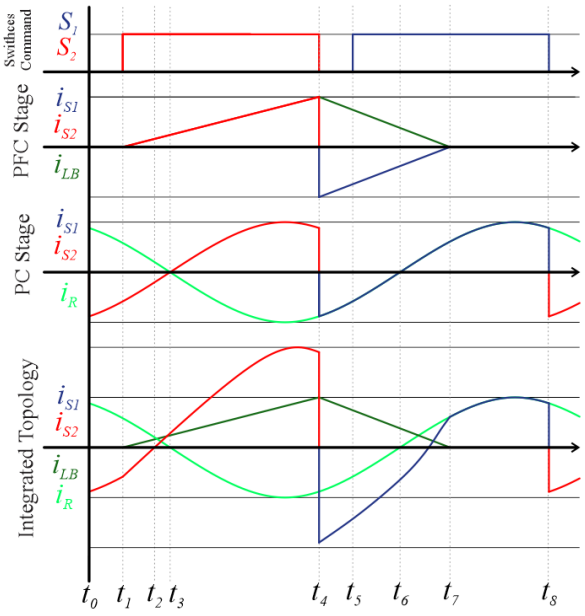


Fig. 4. Waveforms of the integrated topology.

III. PFC AND PC DESIGN

In order to simplify the design procedure, PFC and PC stages design will be developed separately.

A. Boost PFC Bridgeless Totem-Pole Converter

As shown in Fig. 1(c), the boost bridgeless totem-pole PFC converter is constituted of two diodes (D_{R1}, D_{R2}) and two switches (S_1, S_2). These two switches operate in a complementary form. However, even presenting a different structure, the bridgeless totem-pole PFC stage follows the same design as for the conventional boost PFC converter, shown in Fig. 1(a) [23].

By this way, the converter design begins with defining a current conduction mode. As defined in all those reviewed integrated topologies, the DCM is widely used because it has many advantages for PFC converters when compared to other current conduction modes, like less voltage stress and control simplicity. This DCM characteristic was chosen aiming integration simplicity.

Seeking for an UIV, the PFC stage control changes its duty cycle in order to maintain a constant bus voltage. However, to ensure DCM operation over the UIV, the converter operating duty cycle has to be lower than the critical one, which is defined by [23] (1).

$$D_{MAX} = 1 - V_{PK} / V_{BUS} \quad (1)$$

Where: D_{MAX} is the critical duty cycle, V_{PK} is the peak value of the input voltage and V_{BUS} is the PFC stage output voltage or bus voltage of the integrated topology.

In order to elucidate the design procedure, Table I presents the PFC converter design parameters.

Once adopted V_{BUS} = 500 V (justified at the end of the PFC design procedure), the critical duty cycle is calculated for the maximum input voltage (265 V_{RMS}), yielding D_{MAX} = 0.25. To ensure DCM operation at $V_{IN.MAX}$, D = 0.15 is adopted. Following, the boost inductance L_B is determined by (2) [24].

$$L_B = \frac{D^2 T_S}{P_{OUT} T_r} \int_0^{\frac{T_r}{2}} V_{IN}(t)^2 \left(1 + \frac{V_{IN}(t)}{V_{BUS} - V_{IN}(t)} \right) = 232{,}3\mu H \quad (2)$$

TABLE I. PROJECT PARAMETERS: PFC CONVERTER

Symbol	*Parameter*	*Value*
P_{OUT}	Output Power	100 W
V_{IN}	Input Voltage	85 V – 265 V
V_{OUT}	Output Voltage	500 V
f_S	Switching Frequency	102.7 kHz
f_r	Grid Frequency	50 – 60 Hz

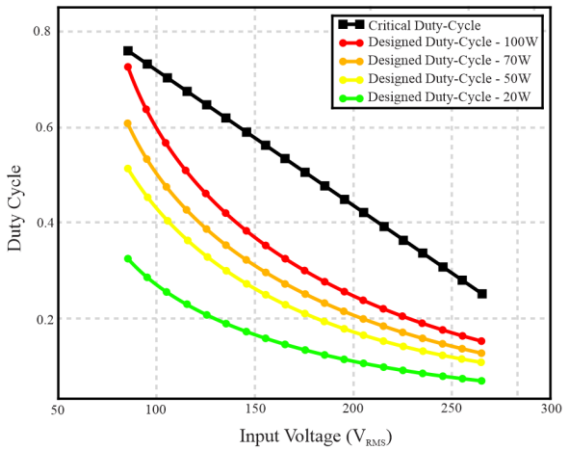


Fig. 5. Plot of D x Vin with output power variation.

Where: D is the adopted duty cycle value for maximum input voltage, T_S is the switching period and T_r is the input voltage period.

Solving (2) for D, the required duty cycle to maintain V_{BUS} = 500 V over the input voltage variation and power variation is obtained. Fig. 5 shows the plot of D (V_{IN}, P_{OUT}) in comparison to D_{MAX}. As it can be seen, DCM is ensured over the UIV variation for different load conditions.

The final design step consist in the estimated PF assesment. The estimated PF for the boost PFC operatin in DCM is given by (3). In this way, employing the design converter parameters and designed L_B, Fig. 6 shows the PFC for different bus voltages.

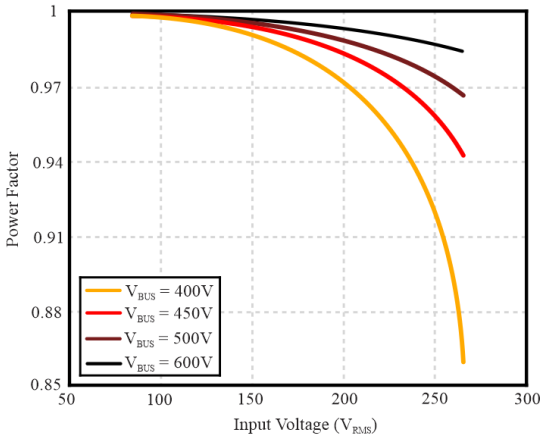


Fig. 6. Plot of PF x V_{IN} with bus voltage variation.

$$PF(V_{IN},V_{BUS}) = \frac{\frac{1}{T_r}\int_0^{T_r} V_{IN}(t)\cdot\left[\frac{D^2}{2L_B f_s}\frac{V_{IN}(t)}{1-\frac{V_{IN}(t)}{V_{BUS}}}\right]dt}{V_{IN\_RMS}\sqrt{\frac{1}{T_r}\int_0^{T_r}\left\{\frac{V_{PK}D^2}{2L_B f_s}\left[\frac{\sin(t)}{1-\frac{V_{IN}(t)}{V_{BUS}}}\right]\right\}^2 dt}} \quad (3)$$

V_{BUS} = 500 V was selected, since this value ensure good PF for all input voltages. If a low bus voltage is choose and it denigrates the PF, the designer can go back to the beginning and adopt higher bus voltage.

B. LLC Resonant Converter

The design is based in the procedure developed in [25] and [26]. Table II shows the LLC resonant converter parameters, and LED piece-wise linear circuit model [7].

TABLE II. PROJECT PARAMETERS: PC CONVERTER

Symbol	*Parameter*	*Value*
P_{OUT}	Output Voltage	100 W
V_{BUS}	Bus Voltage	500 V
f_{SW}	Switching Frequency	102.7 kHz
V_{LED}	LED Terminal Voltage	87.4 V
I_{LED}	LED Current	1.15 A
r_d	Dynamic Resistance	6.219 Ω
V_{th}	Threshold Voltage	80.22 V

Given the design specifications, the transformer turns ratio is defined through (4) [25].

$$n = \frac{V_{BUS}}{2V_{LED}} \quad (4)$$

Considering the employed IRF840 with C_{OSS} = 200 pF and defining t_d = 200 ns, the magnetizing inductance is defined in (5).

$$L_M = \frac{t_d}{16 f_S C_{OSS}} = 608.4\mu H \approx 600\mu H \quad (5)$$

In LLC converter, parameters like λ (ratio between series and magnetizing inductance) and Q (quality factor of the LLC filter) interferes in the resonant filter characteristics Developing the Q and λ analysis likewise in [24] and [25], Q = 3 and λ = 3 is adopted, ensuring enough peak current gain, ZVS and small switching frequency variation over the output load variation. Through the inductance ratio, the series inductance and the series capacitor are calculated, respectively, by (6) and (7).

$$L_S = \frac{L_M}{\lambda} = 200\mu H \quad (6)$$

$$C_S = \frac{1}{4\pi^2 L_S f_S^{\,2}} = 12nF \quad (7)$$

The switching frequency was chosen 102.7 kHz because of rounding. If another frequency was implemented instead, the series capacitor value could not be a commercial value of capacitor, in this case, 12 nF.

Moreover, considering η = 85 %, bus voltage ripple of ΔV_{bus} = 5 % and output voltage ripple ΔV_{LED} = 0.25 %, the bus capacitor and the output capacitor can be designed, respectively, by (8) and (9) [27].

$$C_{bus} = \frac{P_{in}/\eta}{2\pi f_R V_{bus}\Delta V_{bus}} = 24.97\mu F \approx 30\mu F \quad (8)$$

$$C_O = \frac{0.21 I_{LED}}{2\Delta V_{LED} f_S} = 5.381\mu F \approx 10\mu F \quad (9)$$

The LLC transfer function is calculated by two forms (10) (11).

$$H_S = \frac{v_{ac1}}{v_{ab}} = \frac{2n\left(V_{th} + r_d I_{LED}\right)}{V_{BUS}} \quad (10)$$

$$H_S = \frac{\frac{j\omega L_M R_{ac1}}{j\omega L_M + R_{ac1}}}{j\omega L_S + \frac{1}{j\omega C_S} + \frac{j\omega L_M R_{ac1}}{j\omega L_M + R_{ac1}}} \quad (11)$$

Which: $R_{ac} = \frac{8n^2 r_d}{\pi^2}\left(\frac{V_{th} + r_d I_{LED}}{r_d I_{LED}}\right)$.

Matching (10) and (11) and solving the equation for L_S, equation (12) is obtained, which define the required L_S to obtain specific I_{LED}. It is worthy to mention that this equation is valid only for D = 0.5.

$$L_S(I_{LED}) = \frac{\frac{1}{j\omega C_S} + \frac{j\omega L_M 4n\left[2n\left(V_{th} + r_d I_{LED}\right) - V_{BUS}\right]}{j\omega L_M \pi^2 I_{LED} + 8n^2\left(V_{th} + r_d I_{LED}\right)}}{j\omega} \quad (12)$$

In order to show the feasibility of (12), Fig. 7 shows the output current variation as a function of L_S, comparing simulation and theoretical results. By this way, the series inductance can be changed to acquire output current controllability.

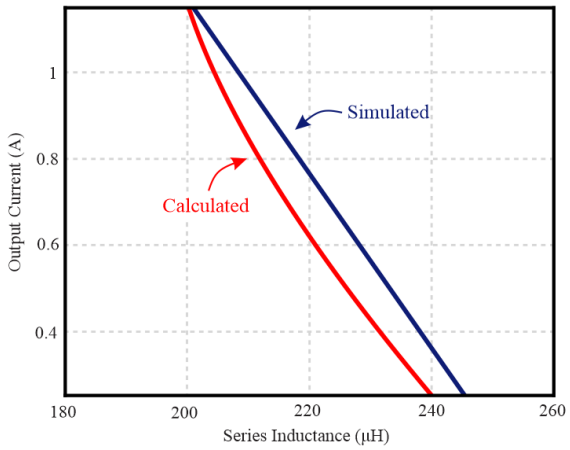


Fig. 7. Graph L_S x I_{LED} with output current variation.

While the bus voltage is controlled by the PFC stage through duty cycle variation, the output current is controlled by the PC stage through a variable series inductor. Nevertheless, the calculated series inductance considers just one operating point (D = 0.5). As the duty cycle variates according the input voltage, this same duty cycle variation affects the resonant converter, requiring further mathematical analysis to define L_S in cases where D ≠ 0.5. The consideration of the C_{DS} capacitor in the simulation can explain the difference between the calculated and simulated curves.

Besides, it is important to emphasize that the converter purposes an integrated system operating asymmetrically. Therefore, First Harmonic Approximation (FHA) analysis may cause undesired errors in the final results.

As an alternative, simulation analysis is carried out in order to define the L_S range necessary to maintain the output current controlled for D ≠ 0.5.

IV. Experimental Results

In order to verify the theorical analysis presented, a 100 W prototype was developed and tested. Once the duty cycle D controls the bus voltage, it is needed to define the series inductance L_S to obtain variable output current. In this way, a simulation analysis was developed. Table III shows the duty cycle needed to obtain V_{BUS} = 500 V for each output power level, as well as the output current considering the designed L_S = 200 µH and the series inductance needed to obtain nominal output current.

TABLE III. Simulation Results

Input Voltage	*P_{OUT}*	*Duty Cycle (V_{BUS} = 500V)*	*I_{LED} (L_S = 200 µH)*	*L_{VAR}*	*I_{LED} (L_S = L_{VAR})*
85 V	100 W	0.724	1.13 A	199 µH	1.15 A
	20 W	0.324	1.36 A	346 µH	0.23 A
120 V	100 W	0.484	1.17 A	201 µH	1.15 A
	20 W	0.217	0.772 A	329 µH	0.23 A
220 V	100 W	0.211	0.735 A	162 µH	1.15 A
	20 W	0.095	0.162 A	157 µH	0.23 A
265V	100 W	0.15	0.39 A	108 µH	1.15 A
	20 W	0.067	0.082 A	85 µH	0.23 A

Fig. 8 shows the variable inductor curve considering the limits of the designed inductance shown in Table III, as well as the implemented variable inductor.

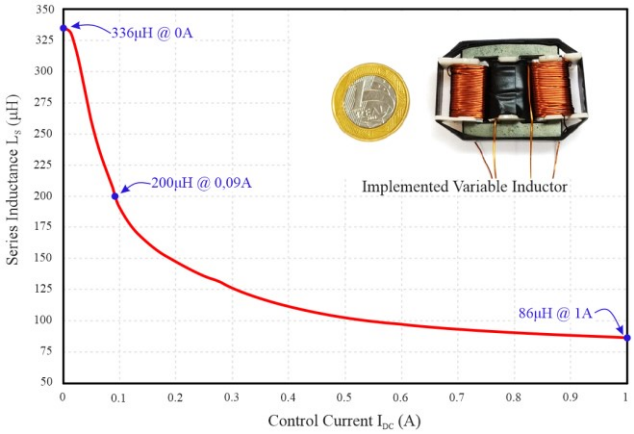


Fig. 8. Variable inductor small-signal characteristic and its implementation.

Fig. 9 shows in details the circuit including duty cycle and L_S control. To implement the digital system, the MCU TM4C1294NCPDT from Texas Instruments is used. L_f = 2,262 mH and C_f = 106,1 nF were designed to filter the input current.

The analog synchronism circuit is employed to detect when the input voltage is positive or negative. Once defined the half cycle's signal, the switches S_1 and S_2 can operate concomitantly.

Fig. 10(a) and Fig. 10(b) show input voltage and current waveforms, bus voltage, output voltage, output current and ZVS achieving for V_{IN} = 85 V, considering P_{OUT} = 100 W and P_{OUT} = 20 W, respectively. These results are obtained through a complete circuit simulation. In these cases, ZVS is achieved in both switches, as well adequate bus voltage and output current regulation.

Subsequently, Fig 11(a) and Fig. 11(b) show the same voltage and current measurements, as well ZVS achieving for V_{IN} = 265 V, considering P_{OUT} = 100 W and P_{OUT} = 20 W, respectively. ZVS is lost in switch S_2 for high input voltage, due to low current amplitude when S_2 turns on. However, adequate bus voltage and output current regulation are obtained. A thorough analysis of the operation is needed to achieve ZVS in all operating points.

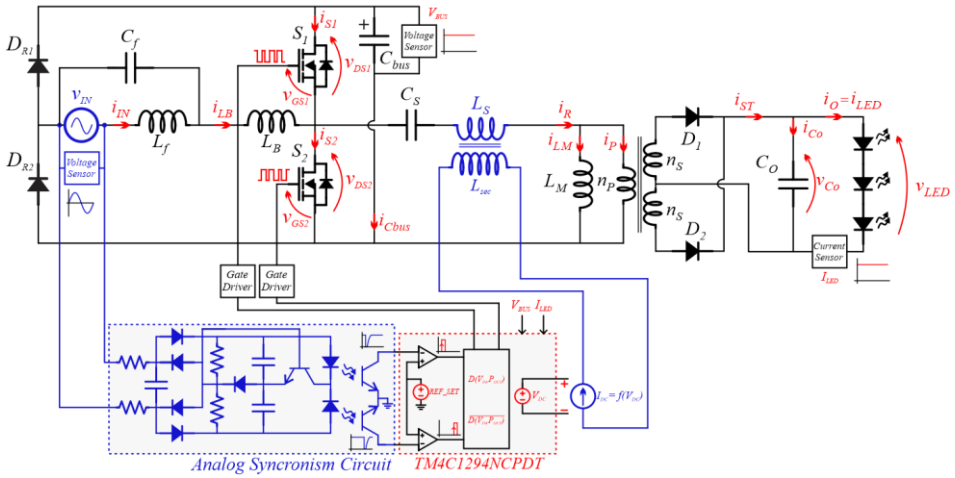


Fig. 9. Circuit incluiding D and L_S control.

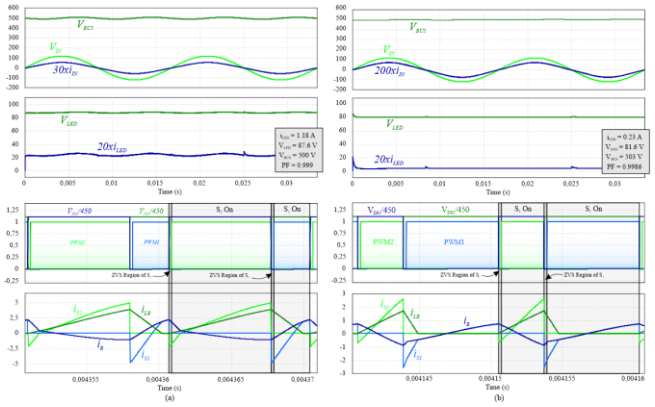


Fig. 10. Input voltage and current waveforms, bus voltage, output voltage and current and ZVS achieving in simulation. (a) P_{OUT} = 100 W. (b) P_{OUT} = 20 W.

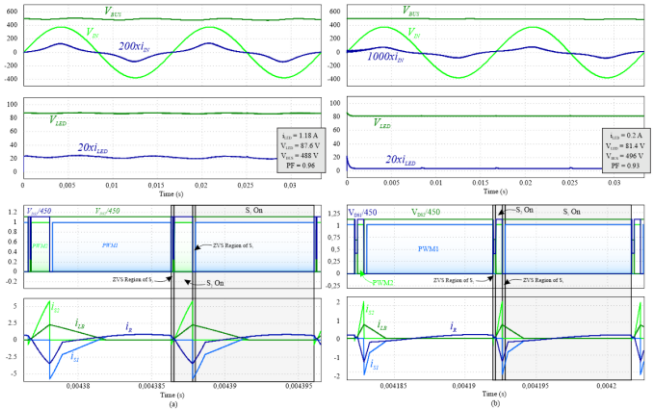


Fig. 11. Input voltage and current waveforms, bus voltage, output voltage and current and ZVS achieving in simulation. (a) P_{OUT} = 100 W. (b) P_{OUT} = 20 W.

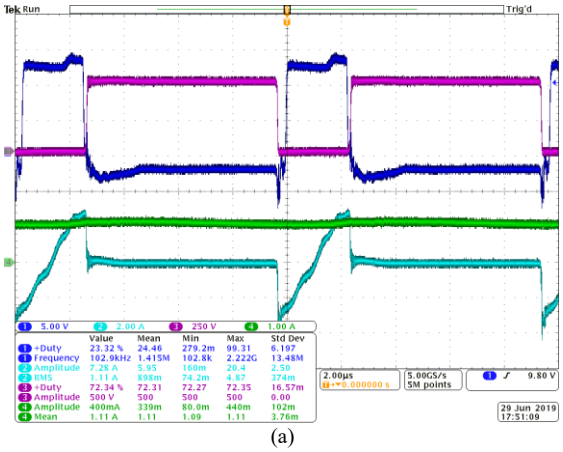
The integrated converter was implemented through a 100 W LED driver. The components list used on the implemented converter are shown in Table IV.

Fig. 12(a) shows experimental results, where is shown the current and voltage waveforms for S_1, as well as current and voltage waveforms for S_2 are shown in Fig. 12(b). These results are obtained considering V_{IN} = 85 V and P_{OUT} = 100 W. The measured output current is near to nominal (1.11 A) and bus voltage is 500 V, approximately. ZVS feature is achieved in both switches, once the current flowing through them is negative when they are turned on.

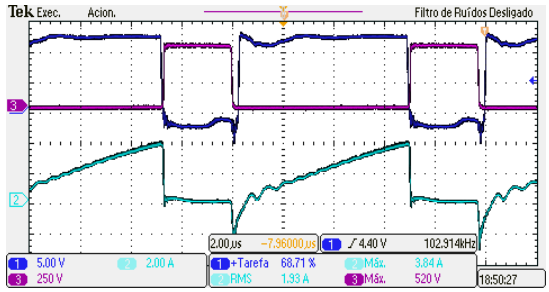
Fig. 13 shows current and voltage waveforms considering V_{IN} = 85 V and P_{OUT} = 20 W. In this operating point the ZVS feature is lost in the switch S_2, once the amplitude current when S_1 turns off is very low and the intrinsic diode of S_2 does not conduct current.

TABLE IV. COMPONENTS USED ON THE INTEGRATED CONVERTER

Symbol	*Component*	*Symbol*	*Component*
D_{R1}, D_{R2}	MUR260G	C_S	12 nF
C_f	106.1 nF	L_S	86 µH – 336 µH
L_f	2.262 mH	L_M	600 µH – 34:12
L_B	232.3 µH	D_1, D_2	SB3200TA
S_1, S_2	STP21N90K5	C_o	10 µF – 100V_{DC}
C_{bus}	30 µF – 700V_{DC}	LED	3 x BXRC-50C4000-F-04

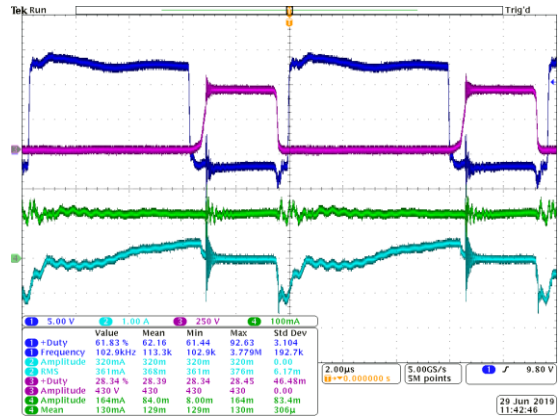


(a)

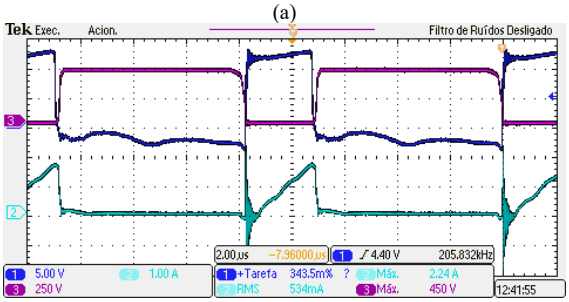


(b)

Fig. 12. Current and voltage waveforms in the switches for V_{IN} = 85 V and P_{OUT} = 100 W @I_{DC} = 0.1A. (a) CH1- V_{GS1}; CH2 - i_{S1}; CH3 - V_{DS1}; CH4 - i_{LED}. (b) CH1 - V_{GS2}; CH2 - i_{S2}; CH3 - V_{DS2}. Scales on the picture.



(a)



(b)

Fig. 13. Current and voltage waveforms in the switches for V_{IN} = 85 V and P_{OUT} = 20 W @I_{DC} = 0 A. (a) CH1- V_{GS1}; CH2 - i_{S1}; CH3 - V_{DS1}; CH4 - i_{LED}. (b) CH1 - V_{GS2}; CH2 - i_{S2}; CH3 - V_{DS2}. Scales on the picture.

The experimental results for input voltage of 265 V are not shown, once ZVS feature is lost in the switch S_2 for operating points with high input voltage. In these operating points, the duty cycle adopted is very low. Defining limits of duty cycle (0.3 – 0.7, for example) and accepting bus voltages variations (450 – 550 V, for example) may be a way to solve the ZVS problem in the switch S_2.

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VI. CONCLUSION

This paper has presented a LED driver based on an integration between a boost bridgeless totem-pole converter operating as PFC stage and an LLC resonant converter operating as PC stage. The main objective of this paper aims obtaining UIV and dimming in a single-stage LED driver. It was achieved varying duty cycle in PFC stage to obtain constant bus voltage and implementing a variable inductor in PC stage to obtain controlled output current. This single-stage achieves great bus voltage regulation and appropriate dimming in simulation results, considering UIV. The experimental result shows the ZVS characteristic for one operating point. This attribute is responsible, mostly, for reducing the power losses associated with the LED driver and, moreover, achieving high PF and great efficiency. It is important emphasize that this integrated topology does not interferes in voltage stress of the switches sharing, as usually happens with integrated converters. The integrated topology demonstrated a great performance, where both converters functionality is not affected by the integration. However, further mathematical and simulation analysis are needed, in order to obtain ZVS in both switches for all operating points. It is important standing out the great controllability, achieving stable bus voltage and dimming.

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