SYNCHRONOUS ZETA POL TOPOLOGY DC-DC CONVERTER MODELING FOR VOLTAGE REGULATION APPLICATIONS OF HIGH EFFICIENCY

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Abstract— This paper reports the Zeta DC-DC converter modeling considering the expressive losses in its components. The procedure is detailed and a voltage regulator for portable appliances is specified and the designed converter is analyzed. The modeling strategy allows the design to be closer to the specifications indicating the design feasibility regarding the converter gain and efficiency. The diode forward voltage versus the device power loss is deeply analyzed. The design issues are exposed in a way a synchronous Zeta in Point-of-Load converter was proposed to fulfill the application minimum requirements.

Keywords— Zeta, Point-of-Load, DC-DC converter, Losses modeling, Efficiency analysis

Resumo— O presente artigo aborda o modelo de conversor CC-CC de topologia Zeta considerando as perdas expressivas em seus componentes. O procedimento de projeto e modelagem é detalhado e uma aplicação de regulação de tensão é proposta. A estratégia de modelagem permite que o projeto seja mais próximo das especificações, indicando a viabilidade do projeto em relação ao ganho e eficiência do conversor. A tensão de condução do diodo, em relação às perdas intrínsecas do dispositivo, é analisada. Logo, com base nas deficiências da topologia, um conversor Zeta em ponto-de-carga síncrono é proposto para atender os requisitos mínimos da aplicação.

Palavras-chave— Zeta, Ponto-de-carga, Conversor CC-CC, Modelagem de perdas, Análise de eficiência

1 INTRODUCTION

Since the 70's, the semiconductor technology has been deeply explored and studied intensively, allowing the development of modern devices such as: power MOSFET, GaN-FET and SiC. (Yano et al., 2004). Once the efficient switching is a crucial item in power electronics, the switches must be carefully chosen in every power circuit.

In general, there are four possibilities for a power system configuration relating the circuit inputs to its outputs: DC-DC (converter), AC-DC (rectifier), DC-AC (inverter) and AC-AC (cycle-inverter) circuits (Erickson and Maksimovic, 2001). These circuits compose different stages of power-sources, computers, cellphones, portable audio systems, fluorescent lamps, distributed generation circuits, among other electronic applications.

The Zeta topology is a buck-boost DC-DC converter, in which the output voltage has a low ripple magnitude for relatively small passive components. Down sizing is a challenging target in power electronics converters design, because size reduction generally means cost reduction and low-cost components usually lowers the circuit overall efficiency. To achieve higher levels of efficiency in such conditions, individual converters with improved performance close to their point-of-load (POL) has been adopted as the secondary stage of Distributed Bus Architecture (DBA) low output voltage power supply circuits (Brown, 2002).

In this paper the efficiency and static gain in terms of component intrinsic losses are meticulously studied. A specific application using the Zeta topology is proposed in which the circuit is deeply analyzed.

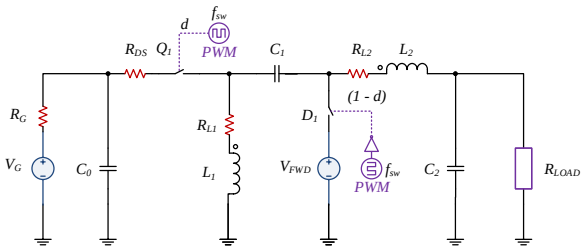

Figure 1: Zeta converter topology

Therefore, the standard Zeta topology efficiency is discussed and based on the proposed model, a synchronous Zeta POL converter is designed to improve the circuit performance and work around the efficiency issues of the traditional topology.

2 ZETA CONVERTER MODELING

The Zeta DC-DC converter is shown in Figure 1. The output voltage and current have low ripple for relative small components, being one of the great advantages of this topology (Falin, 2010).

In this proposed modeling, the expressive losses were taken into account, allowing the hardware designer to specify the components more precisely and foresee other any hardware requirements. So, all the equivalent series resistances (ESR) were added in the components individual model for the following Kirchoff's analyses (1) and (2).

Once the circuit is non-linear, the switched system has two states of operation for continuous conduction mode (CCM): on and off (Rogers, 1999).

The circuit equations related to the period of time

when the controlled switch is on, are in conformity to (1).

$$\begin{cases} v_{L1} = v_{C0} - R_{L1} \cdot i_{L1} - R_{DS} \cdot (i_{L1} + i_{L2}) \\ v_{L2} = v_{C0} - v_{C1} - v_{C2} - R_{L2} \cdot i_{L2} - R_{DS} \cdot (i_{L1} + i_{L2}) \\ i_{C0} = -\frac{v_{C0} - v_G + R_G \cdot (i_{L1} + i_{L2})}{R_G} \\ i_{C1} = i_{L2} \\ i_{C2} = i_{L2} - i_{RLOAD} \\ v_{Q1} = R_{DS} \cdot (i_{L1} + i_{L2}) \\ i_{Q1} = i_{L1} + i_{L2} \\ v_{D1} = v_{C0} - v_{C1} - R_{L1} \cdot i_{L1} \\ i_{D1} = 0 \end{cases} \tag{1}$$

When the controlled switch is off, the Kirchoff's expressions for all the components are described in (2).

$$\begin{cases} v_{L1} = v_{C1} - V_{FWD} - R_{L1} \cdot i_{L1} \\ v_{L2} = -V_{FWD} - v_{C2} - R_{L2} \cdot i_{L2} \\ i_{C0} = -\frac{v_{C0} - v_G}{R_G} \\ i_{C1} = -i_{L1} \\ i_{C2} = -\frac{v_{C2} - R_{LOAD} \cdot i_{L2}}{R_{LOAD}} \\ v_{Q1} = V_{FWD} - v_{C1} + v_G + R_{L1} \cdot i_{L1} \\ i_{Q1} = 0 \\ v_{D1} = V_{FWD} \\ i_{D1} = i_{L1} + i_{L2} \end{cases} \tag{2}$$

3 STATE-SPACE MODEL

After we have obtained all the Zeta converter Kirchoff's equations, the circuit can be modeled from the bilinear approach and represented in the state-space form (3) (Erickson and Maksimovic, 2001):

$$\begin{cases} \dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \\ \mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{E}\mathbf{u} \end{cases} \tag{3}$$

The vector "**x**" represents the state variables, "**u**" the inputs, "**y**" the outputs and d is the duty-cycle. The vectors are a composition of an average (capital letter) and a ripple term represented with a tilde (4).

$$\mathbf{x} = \mathbf{X} + \tilde{\mathbf{x}}, \qquad \mathbf{u} = \mathbf{U} + \tilde{\mathbf{u}}, \qquad \mathbf{y} = \mathbf{Y} + \tilde{\mathbf{y}}, \qquad d = D + \tilde{d} \tag{4}$$

Ignoring the second order terms, the average values of the state variables can be achieved in the steady-state condition (5).

$$\mathbf{X} = -\mathbf{A}^{-1}\mathbf{B}\mathbf{U} \tag{5}$$

The sum of the average values is null due to the model simplification after proceeding the circuit linearization (Fuzato et al., 2016) (Erickson and Maksimovic, 2001). Based on the set of state-space representation, isolating the terms related to the variable duty-cycle terms, we obtain the state-space in the following system of equations (6):

$$\begin{cases} \dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} + \mathbf{F}\tilde{d} \\ \mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{E}\mathbf{u} + \mathbf{G}\tilde{d} \end{cases} \tag{6}$$

The average output vector "**Y**" can be written in terms of the average input values (7).

$$\mathbf{Y} = -\mathbf{C}(\mathbf{A}^{-1}\mathbf{B}\mathbf{U}) + \mathbf{E}\mathbf{U} \tag{7}$$

Moreover, the matrices **A, B, C, E, F** and **G** can be obtained from equation systems (1), (2) and (6).

Considering:

$$\begin{cases} \sum R = R_G + R_{L1} + R_{L2} + R_{LOAD} + R_{DS} \\ R_\zeta = R_{L2} + R_{LOAD} \\ \Phi = R_\zeta + D^2 \cdot (\sum R - R_{DS}) + 2D \cdot (\frac{R_{DS}}{2} - R_\zeta) \\ D' = 1 - D \end{cases}$$

$$\mathbf{A} = \begin{bmatrix} -\frac{R_{L1} + D \cdot R_{DS}}{L1} & -\frac{D \cdot R_{DS}}{L1} & \frac{D}{L1} & \frac{1-D}{L1} & 0 \\ -\frac{D \cdot R_{DS}}{L2} & -\frac{R_{L2} + D \cdot R_{DS}}{L2} & \frac{D}{L2} & -\frac{D}{L2} & -\frac{1}{L2} \\ -\frac{D}{C0} & -\frac{D}{C0} & -\frac{1}{C0 \cdot R_G} & 0 & 0 \\ \frac{1-D}{C1} & \frac{D}{C1} & 0 & 0 & 0 \\ 0 & \frac{1}{C2} & 0 & 0 & -\frac{1}{C2 \cdot R_{LOAD}} \end{bmatrix} \tag{8}$$

$$\mathbf{B} = \begin{bmatrix} 0 & -\frac{1-D}{L1} \\ 0 & -\frac{1-D}{L2} \\ \frac{1}{C0 \cdot R_G} & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{9}$$

$$\mathbf{F} = \begin{bmatrix} \frac{V_{FWD}}{L1} + \frac{D' \cdot (V_G \cdot R_\zeta + V_{FWD} \cdot (R_\zeta + R_{DS}) - D \cdot V_{FWD} \cdot (\sum R - R_{DS})}{L1 \cdot \Phi} \\ \frac{V_{FWD}}{L2} + \frac{D' \cdot (V_G \cdot R_\zeta + V_{FWD} \cdot (R_\zeta + R_{DS}) - D \cdot V_{FWD} \cdot (\sum R - R_{DS})}{L2 \cdot \Phi} \\ \frac{D' \cdot V_{FWD} - D \cdot VG}{C0 \cdot \Phi} \\ \frac{D \cdot VG - D' \cdot V_{FWD}}{C1 \cdot \Phi} \\ 0 \end{bmatrix} \tag{10}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{11}$$

$$\mathbf{E} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{12}$$

$$\mathbf{G} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{13}$$

In conformity to the equation systems (1) and (2), the matrix **E** is null, then **Y** is equal to **X**.

$$\mathbf{Y} = \mathbf{X} = \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C0} \\ V_{C1} \\ V_{C2} \end{bmatrix} \tag{14}$$

Considering:

$$\begin{aligned} \Gamma = {} & D^2 \cdot (\sum R - R_{DS}) \\ & + 2D \cdot (\frac{R_{DS}}{2} - R_\zeta) \\ & + R_\zeta \end{aligned}$$

Each term of the output matrix can be expressed as in (15).

$$\begin{cases} I_{L1} \cdot \Gamma = & D^2 \cdot V_G - D \cdot D' \cdot V_{FWD} \\ I_{L2} \cdot \Gamma = & D' \cdot D \cdot V_G - D'^2 \cdot V_{FWD} \\ V_{C0} \cdot \Gamma = & D \cdot D' \cdot R_G \cdot V_{FWD} + V_G \cdot [R_\zeta \\ & +2 \cdot D \cdot (\frac{R_{DS}}{2} - R_\zeta) \\ & +D^2 \cdot (R_{L1} + R_\zeta)] \\ V_{C1} \cdot \Gamma = & D^2 \cdot V_G \cdot (R_{L1} + R_\zeta) \\ & -D \cdot D' \cdot V_{FWD} \cdot (R_{L1} + R_\zeta) \\ & +(D' \cdot V_{FWD} - D \cdot V_G) \cdot R_\zeta \\ V_{C2} \cdot \Gamma = & R_{LOAD} \cdot D' \cdot (D \cdot V_G - D' \cdot V_{FWD}) \end{cases} \tag{15}$$

The converter average output voltage is equal to V_{C2} as calculated in (15) and the static voltage gain, H_v, can be expressed as in (16):

$$H_v = \frac{V_{C2}}{V_G} \tag{16}$$

4 APPLICATION SPECIFICATION

In this section we discuss the application requirements for a low ripple voltage regulator with high efficiency that composes a sub-system of a power supply for portable appliances with extended operational lifetime. So, the converter should maintain the output at a pre-determined voltage considering the whole battery's output voltage range.

It is suitable to adopt a buck-boost topology for the mentioned context, once the converter output voltage is rather higher or lower than its input voltage. Thus, the Zeta topology is chosen to fulfill the presented requirements in accordance to Table 1.

It is possible to cite several applications for portable appliances such as: mobile robotics, drones, handheld instrumentation, mobile phones, electronic tablets, smart battery chargers, among others (Ric, 2017b)(Ric, 2017a).

Table 1: Zeta converter operating specifications

Parameter	Value	Unity
V_{input}	$3.0 < V_G < 4.5$	V
V_{out}	3.3	V
$P_{out_{max}}$	5	W
Efficiency min. (η)	0.90	–
Switching frequency (f_{sw})	40	kHz
Output ripple ($\Delta V_{out_{ripple}}$)	$< 0.5\%$	–
Conduction mode	Continuous	–

Table 2: Inductors ratings

Parameter	L1	L2	Unity
L	36	47	μH
R_L	0.025	0.025	Ω
$I_{L_{avg}}$	2.001	1.515	A
$I_{L_{RMS}}$	2.031	1.538	A
$I_{L_{pk}}$	2.601	1.969	A
P_L	0.103	0.059	W

Then, considering the power-supply is composed of one 3.7V Li-Po battery, the Zeta converter shall maintain the output voltage at 3.3V with a maximum ripple of 0.5%. The switching frequency should be equal to 40 kHz. Efficiency should be at least 90% in the entire input voltage range.

The passive components should have a maximum relative peak-to-peak ripple (K) considering: $K_{I_{L1}} = 0.3$, $K_{I_{L2}} = 0.3$, $K_{V_{C0}} = 0.09$, $K_{V_{C1}} = 0.45$ and $K_{V_{C2}} = 0.01$.

Using the equations obtained from Kirchoff's law (2), (1), the average terms (15), the components relative ripples (K) mentioned before, and also according to (Falin, 2008), (Falin, 2010), (Choudhary and Bell, 2011) and (Erickson and Maksimovic, 2001), the components values can be found. The maximum ratings for current and voltages levels can also be determined as indicated in Tables (2), (3) and (4). The parameters were calculated for the worst case, V_G = 3V. The component losses were considered as: $R_{L1} = 25m\Omega$, $R_{L2} = 25m\Omega$, $R_G = 50m\Omega$, $Q_G = 27nC$, $Q_{GD} = 6.1nC$, $R_{DS} = 27m\Omega$ and $V_{FWD} = 0.3V$, for all the simulations and modeling procedure.

5 SIMULATION RESULTS

In this section, we analyze the simulations performed using LTSpice and Matlab softwares. The modeled Zeta converter has its output voltage and current responses to a 3V input step from Matlab compared to the LTSpice's simulations for the same condition. Later, the circuit parameters are checked if they with-

Table 3: Capacitors ratings

Param.	C0	C1	C2	Unity
C	43	10	114	μF
$I_{C_{RMS}}$	0.940	1.884	0.262	A
$V_{C_{RMS}}$	2.901	3.397	3.300	V
$V_{C_{avg}}$	2.899	-3.288	3.300	V
$V_{C_{pk}}$	3.000	-4.767	3.317	V

Table 4: Semiconductor components ratings

Parameter	Q1	D1	Unity
$V_{rev.pk}$	7.996	7.696	V
I_{avg}	2.001	1.515	A
I_{RMS}	2.727	2.373	A
I_{pk}	4.571	4.571	A
P	0.201	0.455	W

stand to all the requirements listed in the previous section in Table 1.

First, the circuit was simulated in LTSpice and compared to the Matlab calculated model. The output voltage behavior was analyzed by comparing the simulation versus the model results in conformity to Figure 2.

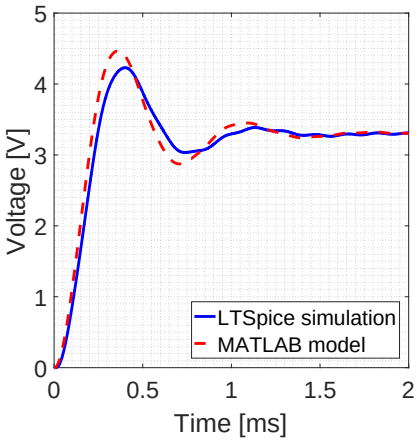

Figure 2: Traditional Zeta converter output voltage simulated in LTSpice and modeled in Matlab

We can see the model has slightly less damping than the simulated circuit response. This is due to the non-ideal switching in simulation and also to the fact the model is more precise for small-signal stimuli.

In addition to that, the duty-cycle had to be slightly adjusted in LTSpice to achieve the sharp output voltage of 3.3V once the simulated circuit has realistic components values. The tuned value for the duty-cycle was 0.581 versus the calculated value of 0.569. So it is noticeable the calculated duty-cycle is

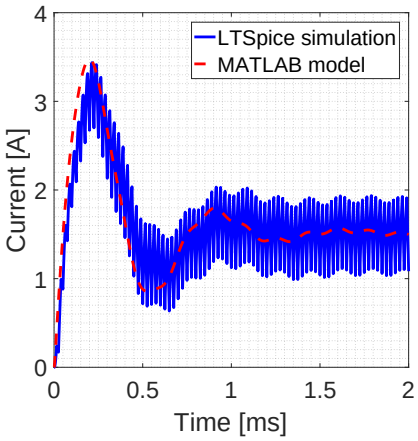

Figure 3: Traditional Zeta converter output current simulated in LTSpice and modeled in Matlab

2.13% lower, due to the circuit linearization. Therefore, the modeled transient behaviors and steady-state values matched the simulated ones.

From Figure 3, we can also notice the modeled output current matches with the simulation result. Once the model was linearized, the non-linear effects noticed from switching components disappears, because only the average terms were taken into account in the modeling procedure.

Moreover, we notice from Figure 4, the circuit operates in continuous conduction mode (CCM). So, the equations and modeling procedures are valid for the proposed circuit passive components values and ripple parameters.

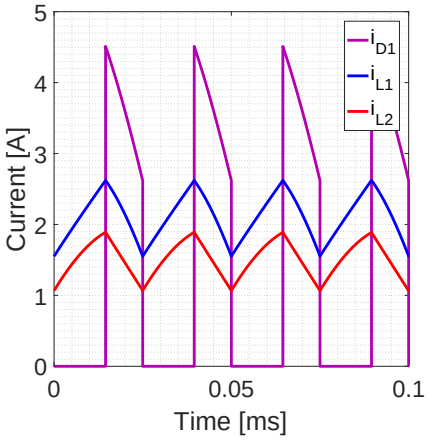

Figure 4: Traditional Zeta converter diode and inductors currents in steady-state simulated in LTSpice for conduction mode verification

The simulation analyses should also cover the output ripple obtained with the passive components chosen. The maximum output voltage ripple should be less than 0.5% in accordance to the application parameters from Table 1. Then, we can notice from Figure 5, the output voltage ripple ($\Delta V_{out_{ripple}}$) is equal to 0.35%.

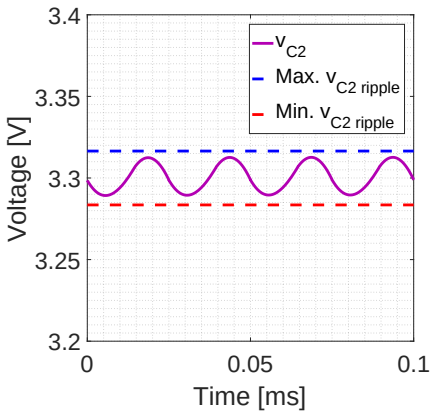

Figure 5: Traditional Zeta converter output voltage ripple in steady-state simulated in LTSpice and the respective application boundaries. Simulated values are: $Max.v_{C2} = 3.313$V, $Min.v_{C2} = 3.290$V and $v_{C2_{pk-pk}} = 22.718$mV

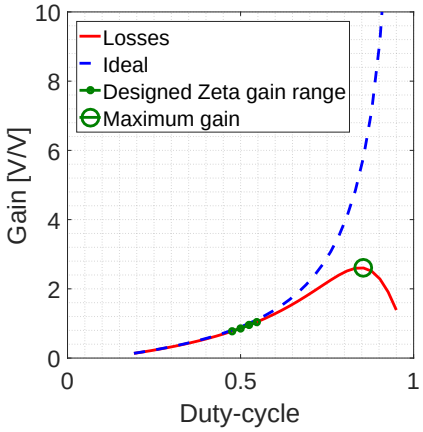

Figure 6: Traditional Zeta gain analysis

Therefore it fulfills the minimum requirements being inside the proposed ripple range.

6 CIRCUIT GAIN AND EFFICIENCY ANALYSIS

In this section, the Zeta converter gain and efficiency are analyzed.

The maximum global and the operational range gain for the traditional Zeta are illustrated in Figure 6. The maximum gain for the proposed losses is equal to 2.602 for a duty-cycle of 0.855.

It can be seen in Figure 6 the higher the duty-cycle, the higher is the influence of the intrinsic losses. However, the designed circuit works under a region the gain behavior is closer to the ideal one.

Table 5: Duty-cycle and gain values obtained for the traditional Zeta converter due to minimum and maximum input voltages

Input (V)	Duty-cycle	Gain (V/V)
3.0	0.5690	1.100
4.2	0.4751	0.786

All the components which has its intrinsic losses considered in the model has its power dissipation analyzed. Then, excluding the battery intrinsic loss (R_G), it is possible to estimate the circuitry overall efficiency independent of the power supply. The obtained losses ratios are described in Table 6.

We notice from Table 6 there is a higher percentage rate of losses over the rectifier D_1 due to its considerable forward voltage level. So, to increase the circuit efficiency it is necessary to decrease the voltage drop through the switch D_1. The lower the voltage drop level, the lower the dissipated power in this device is.

Table 6: Traditional Zeta converter component losses

Component	Power loss (W)	$\mathbf{P_L/P_{total}}(\%)$
$P_{R_{L1}}$	0.103	2.06
$P_{R_{L2}}$	0.059	1.18
$P_{R_{DS}}$	0.201	4.02
$P_{V_{FWD}}$	0.455	9.10

So, based on the Equation (17), it is possible to estimate the maximum voltage drop to achieve an efficiency (η) equal or higher than 90%.

$$P_{D1} = I_{D1_{avg}} \cdot V_{FWD} \tag{17}$$

The maximum dissipation over D_1 should be up to 137mW, so the maximum V_{FWD} should be less than 0.09V.

Nevertheless, this calculated voltage drop is not easily achieved with the standard diodes commercially available. To work around the voltage drop issue, it is feasible to use a power MOSFET N-channel transistor instead the Schottky diode. In this case, the maximum R_{DS} for the device is 60mΩ.

Then, for the configuration in which a MOSFET is employed as the low-side switch, the converter would operate as a synchronous buck-boost converter in its point-of-load (POL) inside the converter highest efficiency operating region.

It is possible to compare the efficiency levels from Figure 8 and gain from Figure 7. Once the gain for the traditional and synchronous Zeta has slightly the same behavior, the duty-cycle operating values for the synchronous Zeta are closer to the Table 5 data.

The circuit efficiency taking into account only the variation of V_{FWD} is illustrated in Figure 9. Therefore, by analyzing Figures 7 and 8, the synchronous Zeta converter operates in its point-of-load in which the efficiency is closer to its maximum value.

Moreover, it can be clearly noticed the converter minimum efficiency is higher than the minimum re-

quirement of 90% for the synchronous Zeta converter.

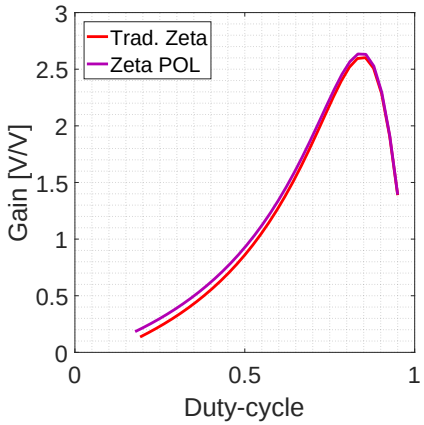

Figure 7: Gain comparison between traditional Zeta and synchronous Zeta POL

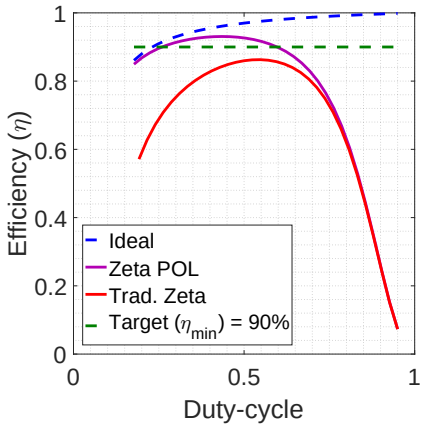

Figure 8: Efficiency comparison between traditional Zeta and synchronous Zeta POL

7 Conclusion

The proposed Zeta topology could be one stage of a power supply with a DBA configuration intended to increase the operational time of a generic mobile, portable or robotic application, because it allows the usage of a single battery cell as the application power source through its whole range of operational voltages.

The Zeta DC-DC converter can supply a low ripple voltage to several 3.3V micro-controllers. Then, the higher the current, more important the analysis of the intrinsic component losses impact is. This analysis is crucial to assure the voltage loss along the circuit can be mitigated by changing the duty-cycle switching ratio to a feasible value.

The modeling strategy allowed the circuit to be successfully designed and fulfilled the proposed application requirements. The Zeta converter achieved

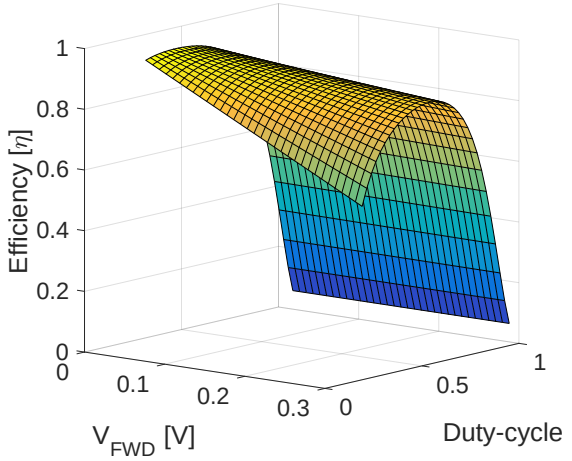

Figure 9: Efficiency analysis versus V_{FWD} variation only

a maximum output voltage ripple of 0.0136V, which represents 0.35% of the respective output voltage, being less than 0.5%. In addition to that, the efficiency boundary for the application conditions considering the usage of a Schottky diode as the low-side switch were reached.

Then it was analyzed the impact of the D_1 device voltage drop in the overall circuit efficiency. This was the most crucial investigation to increase the circuit efficiency. After the analysis, it was concluded another device should be chosen to fulfill the minimum circuit efficiency requirement of 90%.

In this case, to improve the converter performance, a symmetric power MOSFET N-channel with a low R_{DS} should be employed as the low-side switch instead, leading to a synchronous buck-boost POL converter design.

After analyzing the Zeta POL efficiency behavior regarding the duty-cycle operating range, it was observed the circuit successfully fulfilled the application minimum requirements. The LTSpice and Matlab simulations revealed a positive result for the passive components: inductors and capacitors already chosen.

This study enhances the power electronics modeling and design techniques.

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