SPACE VECTOR PWM NINE SWITCH CONVERTER TOPOLOGY.

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Abstract— This article proposes a three-phase inverter topology with nine ac-ac switches, with sinusoidal inputs, unit power factor and low cost due to the reduced number of active switches. Pulse width modulation (PWM) techniques can be used for output voltage, such as triangular modulation or vector modulation. The proposed modulation for the inverter is designed to calculate the optimum operating point based on the specifications of maximizing the DC-link voltage while minimizing output voltage and switching losses (THD). The study of the vector technique uses the DC-link voltage more efficiently, generating smaller harmonic distortions when compared to other techniques. Relevant expressions, application requirements, and simulation results are presented for case identification where the nine-switches inverter can have improved performance.

Keywords— PWM, Space Vector, THD, Topologies, Nine Switch.

Resumo— Este artigo propõem uma topologia de inversor trifásico com nove chaves ac-ac, com entradas senoidais, fator de potência unitária e baixo custo devido ao numero reduzido de chaves ativas. Técnicas de modulação de largura de pulso (PWM) podem ser usada para a tensão de saída, como a modulação triangular ou modulação vetorial. A modulação proposta para o inversor é projetado para calcular o ponto de operação ideal com base nas especificações de maximizar a utilização da tensão do barramento, enquanto minimiza a tensão de saída e perdas de chaveamento (THD). O estudo da técnica vetorial utiliza de forma mais eficiente a tensão do barramento, gerando menores distorções harmônicas quando comparadas a outras técnicas. Expressões relevantes, requisitos de aplicação e resultados de simulações são apresentados para identificação de casos onde o inversor de nove chaves podem ter um desempenho melhorado.

Palavras-chave— PWM, Modulação Vetorial, THD, Topologias, Nove Chaves.

1 Introduction

Three-phase ac/dc/ac and ac/ac converters with variable frequency and variable voltage operation have found wide application in industry. The most popular configuration uses voltage source inverter with a diode rectifier as the front end for adjustable speed drives, uninterruptible power supplies and other industrial applications (Bose, 2009). This type of configuration is inexpensive and reliable operation due to the use of a rectifier diode, but generate highly distorted input line currents and has no regenerative capacity. These problems can be solved by a *Back-to-Back Converter* supply two voltage levels (B2B) shown in Figure 1.

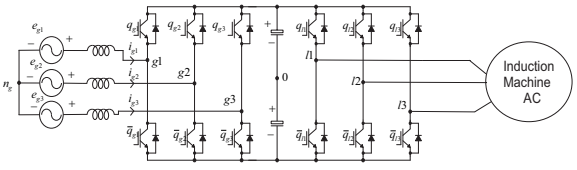

Figure 1: Back-to-Back - 12S

The pulse width modulation - PWM rectifier voltage source is used to replace the diode rectifier. The B2B requires a relatively high number (12) of active switches such as insulated gate bipolar transistors (IGBTs). It also needs a DC-link capacitor that is responsible for a limited lifespan and increased cost. To reduce the device count and minimize the dc-capacitor filter, various converter topologies have been proposed in the literature.

In many applications, a further cost reduction for the drive is an important aspect, and, thus, a reduction of the number of power semiconductors in the converter must be considered (Blaabjerg et al., 1997). The first approach reported in previous papers puts two dc capacitors in cascade and takes their midpoint as one of the input-output terminals, whereby an entire phase leg for the rectifier and/or inverter can be saved (Jacobina et al., 2007) . In addition, combined use of dc midpoint connection and phase leg sharing has been proposed in previous papers, where only four legs (B4)(Figure 2(b)) are needed to perform three-phase ac to ac conversion with bidirectional power flow and power factor control (Jacobina et al., 2006).

It is also possible to reduce the total number of switches, as the second approach suggests by sharing one of the three phase legs between the rectifier and inverter (B5)(Figure 2(a)) with proper control (Jacobina et al., 2006). The performance of this topology is superior to the topologies based on four legs converter, due to a smaller number of switches, the voltage capacity that can be divided between the rectifier and in-

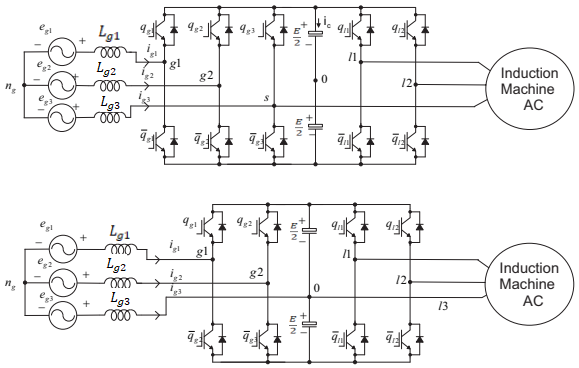

Figure 2: Reduced Switch DC-link Five and Four Leg Converter

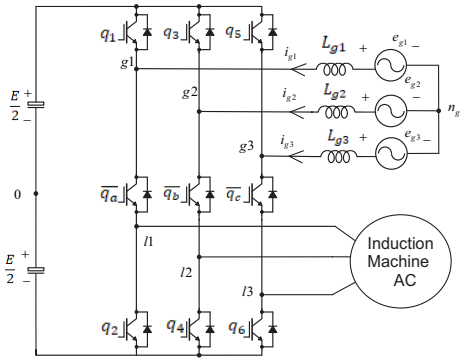

Figure 3: Topology of the nine switch converter.

verter. Moreover, when compared with the converter six legs, five leg converter topology requires less switches at the expense of an increased power level.

Recently, researchers have shown keen interest in the nine switch converter (NSC) shown in Figure 3. It has been used in independent control of two three-phase ac loads (Kominami and Fujimoto, 2007),(Oka and Matsuse, 2007) and in unified power quality conditioners (Zhang et al., 2012). The NSC has also been used to control the doubly-fed induction generator (Soe et al., 2011), permanent-magnet synchronous generator (Heydari et al., 2012) and a six-phase machine drive system (Dos Santos et al., 2011). According to the Figure 3, the top drive comprising the upper and middle switches identified as NSC1 while and the lower portion comprising the middle and lower switches as NSC2.

The NSC topology requires a much higher DC-link voltage to produce the same output voltage compared to the use of two levels of voltage source converters (Oka and Matsuse, 2007), which makes it disadvantageous to use. This limitation is caused by the reduced number of switches that can be overly stressed. Note that the intermediate switches ($\bar{q_a}$,$\bar{q_b}$,$\bar{q_c}$) are shared between NSC1 and NSC2, imposing restrictions that limit the amplitudes and frequencies of the phase voltages to be synthesized. To ensure voltage and current laws are not violated during the Kirchoff operation, NSC1 modulation signals at any instant should always be greater than NSC2 modulation signals.

In this paper, a novel one-stage three-phase ac/ac converter topology is proposed. Different from all other existing topologies, this converter has only three legs with only nine active switches for bidirectional ac/ac power conversion.

The paper is organized in the following order. In Section 2, a detailed nine switch converter topology, in Section 3 modulation techniques for nine switch converter with vector pulse-width modulation in Section 4 simulation is presented, and Section 5 conclusion.

2 Nine Switch Converter Topology

The three-phase nine-switch inverter has only three legs with three switches installed on each of them, which the middle switch is shared by both the rectifier and the inverter, thereby reducing the switch count by 33% in comparison to the B2B. The input power is delivered to the output partially through the middle three switches and partially through a DC-link circuit.

The converter has two modes of operation: constant frequency mode, where the output frequency of the inverter and of the utility supply are constant, while the inverter output voltage is adjustable, which is particularly suitable for applications in uninterruptible power supplies; and variable frequency mode, where both magnitude and frequency of the inverter output voltage are adjustable, applied to variable speed drives. For the nine switch topology, the control of the input and output voltages has to be accomplished through the three switches on each leg. Because the middle switches are shared by the rectifier and inverter, the converter has only three switching states per phase, as listed in Tables 1 and 2. It can be observed that switching state 4 for the B2B does not exist in the nine switch converter, which implies that the inverter leg voltage v_{10} cannot be higher than the rectifier leg voltage v_{20} at any instant. This is, in fact, the main constraint for the switching scheme design of the nine switch converter.

The output voltage of the rectifier is ripple DC, such type of ripples can be eliminated by using the modulation techniques the harmonics also reduced at the inverter output side.

Sates (12S)	q_1	$\bar{q_1}$	q_2	$\bar{q_2}$	v_{10}	v_{20}
1	1	0	1	0	E/2	E/2
2	0	1	0	1	-E/2	-E/2
3	1	0	0	1	E/2	-E/2
4	0	1	1	0	E/2	-E/2

Table 1: Switching States - 12S

Sates (9S) Proposed	q_1	$\bar{q_a}$	q_2	v_{10}	v_{20}
1	1	1	1	E/2	E/2
2	0	1	1	-E/2	-E/2
3	1	0	1	E/2	-E/2

Table 2: Switching States - 9S

In the NSC topology shown in Figure 3, there are 2^9 different possible combinations of all 9 switching devices. However, Kirchoff's current and voltage laws must be obeyed to prevent short-circuiting the DC source and ensure current continuity. Thus, the following constraint on the switching functions must be satisfied:

$$S_{ip} + S_{im} + S_{in} = 2 \quad (1)$$

onde S_{ip}, S_{im} e S_{in} are, respectively, the switching functions of the upper, middle and bottom switching devices and have a value of unity when they are turned-on and take a value of zero when turned-off.

The subscripts $i = a, b, c$ refer to the output phase to which the device is connected; p, m, n refer to the top, middle and bottom devices of the converter leg, respectively. Equation (1) reduces the feasible switching states to twenty seven as shown in Figure 4.

The twenty-seven spatial vectors of the NSI are shown in a spatial representation along with the six active vectors of the VSI. It is worth mentioning that the hexagon of this figure is only an illustrative representation of the spatial vectors of the NSI and can not be used to generate the PWM pulses in the NSI. This representation means that these vectors are graphically equal (on the $\alpha\beta$ axis), however, they represent distinct physical states in the keys.

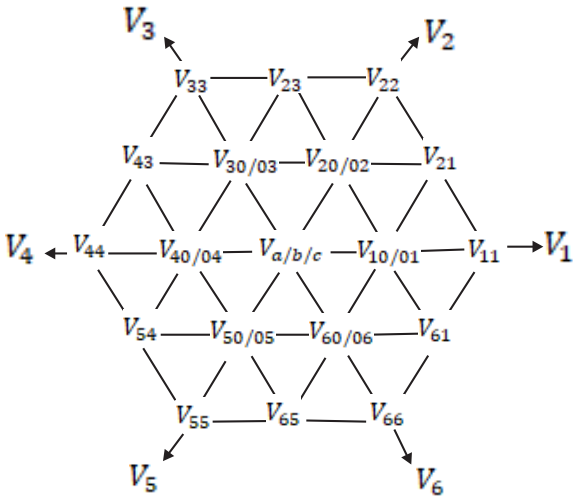

Figure 4: Space representation of the twenty-seven space vectors, along with the six active vectors.

3 Modulation Techniques

In the classical pulse-width modulated voltage source inverters, two main modulation techniques: Space Vector Pulse Width Modulation and Carrier-Based Pulse Width Modulation. In both the methods, voltage linearity, waveform quality, and switching losses are all influenced by the choice of the zero state placement (Holmes and Lipo, 2003). Depending on the placement of these zero vectors, the modulation may be continuous or discontinuous. In Hava (Hava et al., 1998), the continuous PWM methods have superior performance in the low modulation range compared to the discontinuous PWM methods.

For correct functioning of the converter and elimination of the short circuit risk capacitive bus, the three switch of an arm should not be pressed simultaneously, both for the activation of the switch ($\bar{q_a}$,$\bar{q_b}$,$\bar{q_c}$) it depends on the conduction state of the upper switch q_1,q_3,q_5 and lower q_2,q_4,q_6. From the XOR logic of the application - or exclusive - on the trigger signals from the upper and lower switch determines the conduction state of the switch ($\bar{q_a}$,$\bar{q_b}$,$\bar{q_c}$).

The Figure 5 illustrates the generalized modulation scheme in a single switching period for the nine switch converter. The rectifier modulating wave V_{mr} and the inverter modulating wave V_{mi} are arranged such that V_{mr} is not lower than V_{mi} at any instant of time. These two modulating waveforms are compared with a common triangular carrier v_c, in which, the generated rectifier and inverter leg voltages v_{10} and v_{20} are shown. This arrangement guarantees that switch state 4 in the B2B is eliminated here for the nine-switch converter.

By adding 1/2 of the DC voltage to upper reference and subtract the same from the lower reference, selects DC offsets equal to the maximum and the minimum of the phase voltages for upper and lower references.

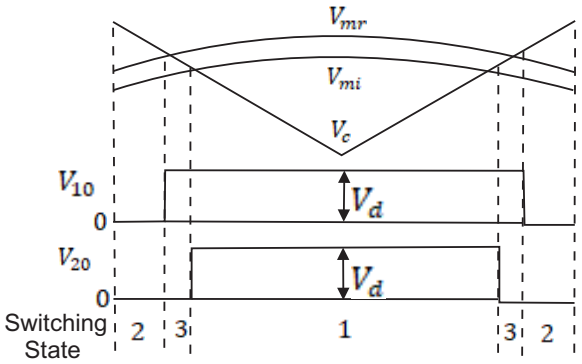

Figure 5: PWM waveform generation.

The Figure 6 shows the block diagram of the PWM strategy employed for the nine switch converter, which V_{offset} is the voltage used to guar-

antee no intersection, in the machine employed.

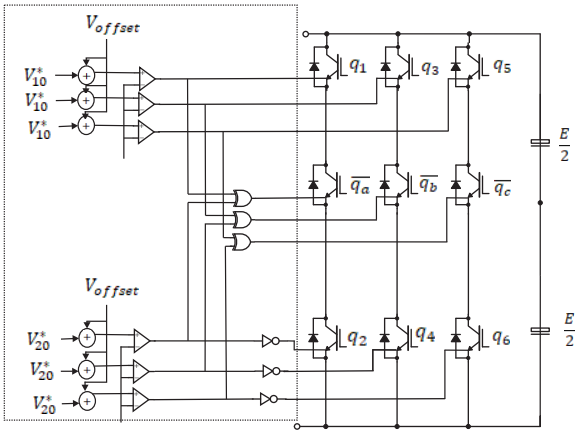

Figure 6: PWM control strategy.

Based on the feasible switching states and equation (1),it perceives that the switching functions of the devices in a leg are related by equation (2):

$$\begin{cases} S_{ip} + S_{im}S_{in} = 1 \\ S_{in} + S_{ip}S_{im} = 1 \end{cases} \tag{2}$$

And the voltages between the converter legs and the midpoint of the dc-link capacitor are given by equation (3), where $j = 1, 3, 5$ and $j = 2, 4, 6$:

$$\begin{cases} V_{j0} = V_{jn} + V_{n0} = \dfrac{E}{2}(2S_{ip} - 1) \\ V_{k0} = V_{kn} + V_{m0} = -\dfrac{E}{2}(2S_{in} + 1) \end{cases} \tag{3}$$

The expressions for the switching functions, in the equation (4), of the top and bottom devices can be obtained from equation (3) and the corresponding modulation signals can be obtained as in equation (6).

$$\begin{cases} S_{ip} = \dfrac{V_{jn} + V_{n0}}{E} + 1/2 \\ S_{in} = \dfrac{V_{km} + V_{m0}}{E} + 1/2 \end{cases} \tag{4}$$

The relationship between the switching functions and the modulated signal is given by:

$$\begin{cases} S_{ip} = \dfrac{(1 + m_{ip})}{2} \\ S_{in} = \dfrac{(1 + m_{in})}{2} \end{cases} \tag{5}$$

Substituting equation (5) into equation (4) results in the following expression for the modulation signals:

$$\begin{cases} m_{ip} = \dfrac{2}{E}(V_{jn}^* + V_{n0}) \\ m_{in} = \dfrac{2}{E}(V_{km}^* + V_{m0}) \end{cases} \tag{6}$$

where m_{ip}, m_{in} are respectively the modulation signals of the upper and bottom devices.

The average neutral voltage can be approximated, if the normalized times are expressed in terms of the line-to-line voltages, and maximum/minimum phase voltages, the generalized neutral voltages after some mathematical manipulations for all possible combinations can be generalized by equation (7).

$$\begin{cases} V_{n0} = \dfrac{E}{2} - V_{max} \\ V_{m0} = \dfrac{E}{2} - V_{min} \end{cases} \tag{7}$$

3.1 Space Vector PWM Technique

The space vector PWM technique is a direct digital PWM method that calculates the conduction times of the switching devices required to synthesize a desired voltage vector. It has been shown that there are 27 feasible switching states of the nine switch converter (Figure 4). The converter voltages in natural abc reference frame can be transformed to the stationary dq reference frame using equation (8):

$$f_{dq0s} = K(\theta) f_{abcs} \tag{8}$$

onde

$$K(\theta) = \frac{2}{3}\begin{bmatrix} cos(\theta) & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ sin(\theta) & sin(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{9}$$

and $f_{dq0s} = [f_{ds} f_{qs} f_{0s}]$, $f_{abcs} = [f_{as} f_{bs} f_{cs}]$ and f_{abcs} may represent voltage, current or flux linkage. The reference transformation angle $\theta = 0°$ for the stationary reference frame (Krause et al., 2013).

To synthesize the desired three-phase voltages, the natural abc voltages are transformed into the qd stationary reference frame voltages using equation (10).

$$\begin{cases} V_{ds}^* = \frac{2}{3}(v_{as} - 1/2v_{bs} - 1/2v_{cs}) \\ V_{qs}^* = \frac{2}{3}(-\sqrt{3}/2v_{bs} - \sqrt{3}/2v_{cs}) \\ V_{0s}^* = \frac{2}{3}(1/2v_{as} + 1/2v_{bs} + 1/2v_{cs}) \end{cases} \tag{10}$$

The corresponding space vector diagrams for switching states are illustrated in Figure 7 and 8.

The following observations can be deduced from the space vector diagrams:

- The zero states of NSC1 and NSC2 are, respectively, {1,14, 15, 17, 18, 23,24, 27} and {1,3,7,9,14,19,21,25,27};
- The zero states {1, 14, 27} are common to both NSC1 and NSC2;
- The remaining zero states {15, 17, 18, 23, and 24} of NSC1 are active states in NSC2 and the zero states {3, 7, 9, 19, 21, and 25} of NSC2 produce active states in NSC1.

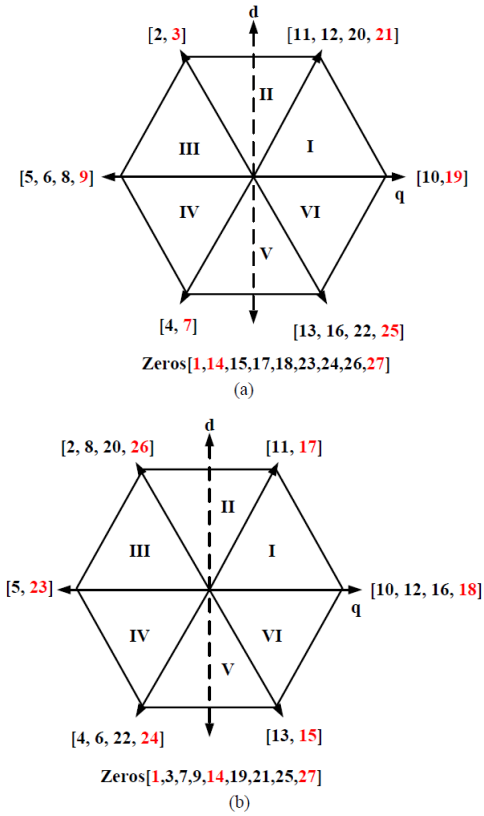

Figure 7: Voltage space vector diagrams for (a) NSC1, and (b) NSC2 for all feasible switching states.

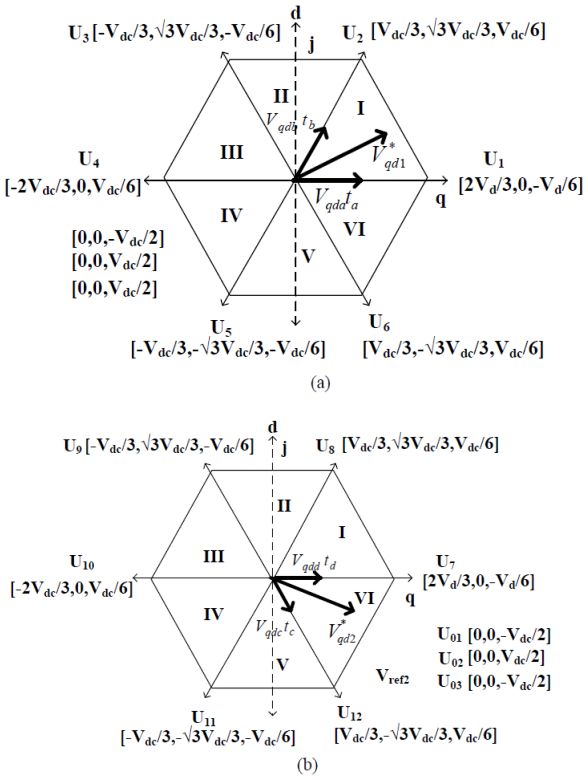

Figure 8: Voltage space vector diagrams for (a) NSC1, and (b) NSC2 for selected switching states which ensures their independent control.

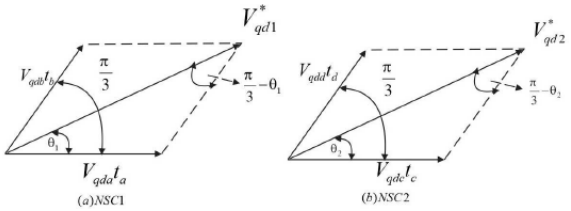

Figure 9: Synthesizing (a) NSC1 and (b) NSC2 reference voltages.

After eliminating the switching states independent control of the converter frequencies is possible since the active states are chosen such that an active state applied to NSC1 produces a zero state in NSC2 and vice versa (Kominami and Fujimoto, 2007). This leaves fifteen permissible states as shown the corresponding space vector diagrams are shown in Figure 8

For voltage, V_1 has the effect of producing an active vector, $V_1[2E/3, 0, -E/6]$ in NSC1 but a zero vector, $V_1[0, 0, -E/2]$ in NSC2, and V_7 has the opposite effect, producing a zero vector, $V_7[0, 0, E/2]$ in NSC1 and an active vector, $V_7[2E/3, 0, -E/6]$ in NSC2. Any two reference three phase voltage sets expressed in the stationary reference frame, V^*_{qd1}, V^*_{qd2} may be synthesized from their immediate adjacent space vectors, V_{qda}, V_{qdb} and V_{qdc},V_{qdd} respectively in addition to the zero vectors V_{qd1} and V_{qd2} as shown in Figure 9.

4 Simulation Results

The implementation of the space vector PWM in MATLAB consists of first identifying the sectors of the desired voltages to be synthesized. The time of application of active and zero vectors are then calculated and arranged according switching pattern. The converter switching frequency chosen is 1kHz and sampling time is $T_s = 20e^{-6}$.

The simulations, the desired two sets of balanced threephase voltages to be synthesized are: $V_{g1} = \frac{50}{\sqrt{3}}cos(2\pi 60t)$,$V_{g3} = \frac{50}{\sqrt{3}}cos(2\pi 60t - 2/3)$ $V_{g5} = \frac{50}{\sqrt{3}}cos(2\pi 60t + 2/3)$ $V_{g2} = \frac{50}{\sqrt{3}}cos(2\pi 30t)$ $V_{g4} = \frac{50}{\sqrt{3}}cos(2\pi 30t - 2/3)$ $V_{g6} = \frac{50}{\sqrt{3}}cos(2\pi 30t + 2/3)$. The DC-link voltage of 100V.

For of the modulation angle, the graphical waveforms of the reference modulation signals are shown in Figure 10. With the modulation signals, the switching pulses can be generated by comparing with high frequency triangular carrier signal.

The Figure 11 and 12 shows all the phase voltages for NSC1 and NSC2 produced using the space vector PWM:

The low frequency components of the synthesized voltages and the reference voltages have been

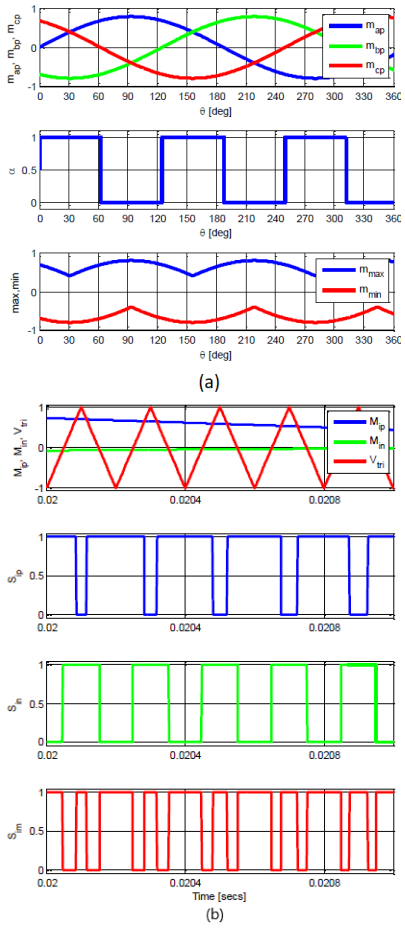

Figure 10: (a) Waveform of the reference modulation signals with $\delta = 30°$ showing the maximum and minimum values in the six sectors; (b) Generation of NSC device gate switching pulses.

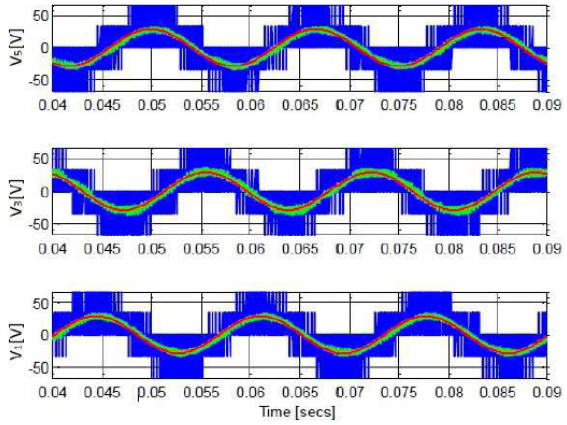

Figure 11: Phase voltages for NSC1 output (f1 = 60 Hz).

superimposed, which shows that, the desired voltages have correctly been synthesized. Figure 13 shows the converter line-to-line voltages.

The Figure 14 depict the corresponding load currents of the converter.

The Figure 15 shows the simulation of the voltage stress on each device in a leg showing that

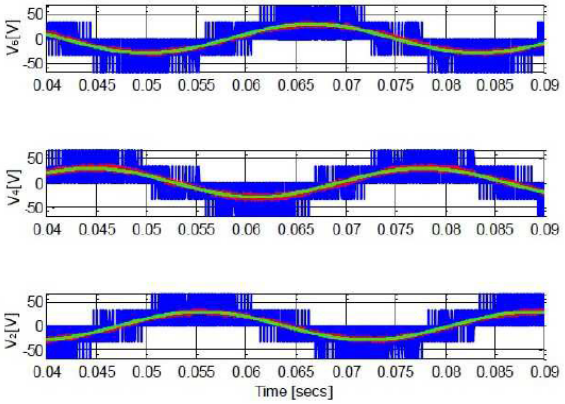

Figure 12: Phase voltages for NSC2 output (f2 = 30 Hz) using Space Vector PWM.

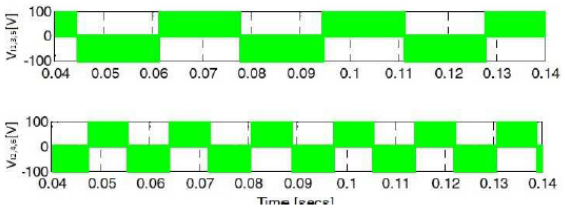

Figure 13: NSC line-to-line voltages with f1 = 30 Hz and f2 = 60Hz.

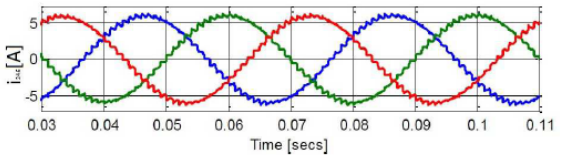

Figure 14: Simulation results of the load currents.

the switching losses per cycle on the middle devices are about twice those of the top and bottom devices.

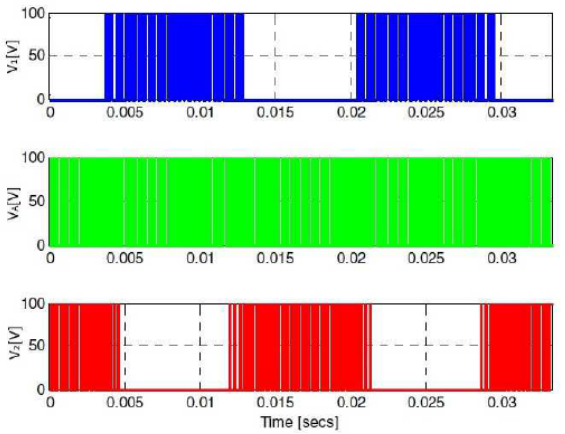

Figure 15: Voltage on devices.

The Figure 16 (a), (b) and (c) show the IGBT conduction losses as functions of the power factor

angle. Fig. 16 show the losses of the top devices. The power factor angle is varied from $-90°$ to $90°$ and the plots show the variation of the total IGBT conduction losses with the power factor angle. It can be shown that the total losses are almost independent of the modulation control angle. The minimum and maximum losses occur at unity power factor leading and unity power factor lagging respectively.

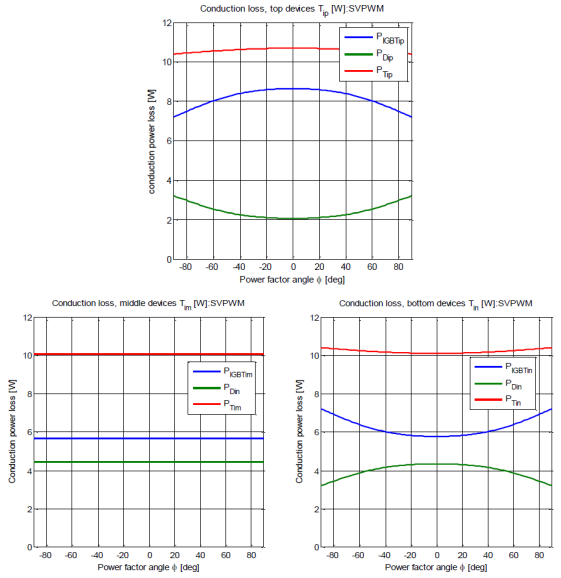

Figure 16: IGBT conduction power losses of the top (a), of the middle (b) and of the bottom (c) devices as a function of the power factor.

It can be shown that when a device is turned-off, the voltage across it is equal to the input DC voltage, E. Thus the condition following combination of switches on all three phases: $S_{1p} = 0$, $S_{2n} = 1$, $S_{3p} = 1$, $S_{4n} = 0$, $S_{5p} = 1$ and $S_{6n} = 1$. Since at any particular switching condition, two switches will be on in one phase, using the per phase truth table, the voltage stress on each device in a leg can be determined in terms of the switching functions, as shown in Table 3.

Sates	Sip	Sim	Sin	Device Voltage
1	0	1	1	$(1 - S_{ip})E$
2	1	0	1	$(1 - S_{ip})E$
3	1	1	0	$(1 - S_{ip})E$

Table 3: Calculating device voltage stress

The %WTHD e %THD for space vector PWM is measured and tabulated as shown in Table 4. To minimize harmonic distortion, active vectors for each output should be placed centrally in the switching period.

Number of switching of semiconductor elements for nines which inverter is shown in Table 5, in which number of switching is considerably reduced using proposed space vector PWM.

	%WTHD	%THD
g_1	45,08	18,03
l_1	45,08	17,07

Table 4: Harmonic Distortion

S_{ip}	3336
S_{im}	2336
S_{in}	3336

Table 5: Number Switch

5 Conclusões

Space vector Modulation Technique has become the most popular and important PWM technique for the control of AC induction, Switched Reluctance and Permanent Magnet Synchronous Motors.

The space vector pulse width modulation methodology for the nine-switch converter are proposed. The topology uses only nine IGBT devises for ac to ac conversion through a DC-link circuit. Simulation results of method space vector - PWM output was discussed. The space vector PWM higher fundamental voltages compared to sine triangle PWM based controllers, also low voltage and current ripples. The operating principle of the converter is discussed and space vector modulation scheme is developed. The performance of the converter topology is verified through simulation.

Although it is technically feasible to share the carrier, it is not favorable in practice, even if it is to produce the same voltage at the output, because it limits the amplitude of the output signals. The voltage of the dc bus is maintained at twice the usual amount, and thus the voltage stress on the semiconductor is at least doubled.

Doubling the voltage is not, however, necessary in the traditional structure, the *back-to-back converter*, and thus also supports the maximum modulation index. The doubling of the dc bus voltage is attributed to a reduction by half of the modulation rates imposed by nine keys converter, and is therefore also experienced by drives of adjustable speed motors ac/dc/ac where the nine keys converter also operates at different frequencies.

6 Agradecimentos

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