DC-LINK CONTROL FOR A FIVE-LEVEL DIODE-CLAMPED INVERTER WITH REDUCED NUMBER OF COMPONENTS

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Abstract— This paper presents a capacitor voltage balancing method for the five-level diode-clamped inverter using level-shifted pulse-width modulation (LS-PWM), including the voltage balancing of DC-link capacitors. The proposed system has a reduced number of components for mitigation of losses. The DC-Link capacitor voltage is regulated by adjusting the switching duty cycles of DC/DC converter. Simulation results are presented to verify the validity of this method.

Keywords— DC-Link voltage balancing circuit, Five-Level NPC Inverter, Coupled Inductors

1 Introduction

Multilevel inverters allow the use of medium power devices in high voltage applications. Since the Cascaded H-Bridge converter arise at the middle of the 1970 many different topologies have been conceived. Besides the NPC converter, other well-investigated multilevel converters are the Neutral Point-Clamped (NPC) inverter (Nabae et al., 1981), the Flying Capacitor (FC) (Rodriguez et al., 2002), and, recently, the Modular Multilevel converters (Lesnicar and Marquardt, 2003) and Hybrid Inverter (Andrade and Muniz, n.d.).

The goal of a multilevel inverter is to generate high quality output waveforms and many topologies, as stated before, has been proposed, including four-level and five-level topologies with a low device count (Kouro et al., 2010; Pan et al., 2004). Fig. 1(a) presents the conventional 5- level NPC half-bridge (Choi et al., 1991). This converter employs four DC-sources, eight switches and six diodes. In fact it has been shown that the devices suffer from unequal voltage stress. Equalization of voltage upon the diodes can be achieved by using more than one diode in series (Peng, 2000), which increases the number of devices. In order to reduce the number of device, as shown in Fig. 1(b), the Diode-Clamped Topology proposed for (Pan et al., 2004) with reduced four diodes in comparison with NPC topology (Andrade et al., 2012).

Some papers in the literature proposes solve the problem of unbalance of DC-link voltages. In (Wang, Xu, Zheng and Li, 2015; Wang, Li, Zheng, Xu and Fan, 2015) the control of the floating capacitor is realized through of modification in the LS-PWM modulation. Other works uses DC/DC converters to control of the DC-link voltages (Narendrababu and Agarwal, 2014; Corzine and Majeetha, 1999). The DC/DC converter proposed by (Corzine and Majeetha, 1999) has fewer components than the converter proposed by (Narendrababu and Agarwal, 2014), however, the converter is used on DC-link for a four-level inverter.

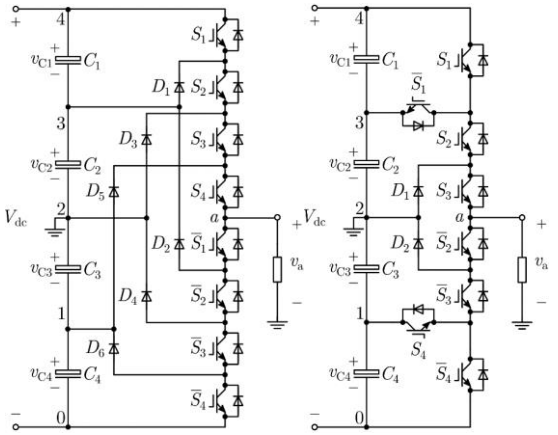


Figure 1. Five-level inverter. (a) NPC (b) DiodeClamped

This paper proposes the DC-link voltage control of the five-level hybrid inverter topology shown in Fig. 1(b) as an alternative to NPC with a reduced number of components. The four-level DC/DC converter proposed by (Corzine and Majeetha, 1999) will be modified on DC-link to furnish the five-level output voltages.

2 Proposed System

The proposed system are shown in Fig. 2. It is a single-phase inverter five-level diode clamped topology with a DC/DC converter to the DC-link voltage control. The output of the converter feeds a RL load. The inverter hybrid topology have a reduced number of components in comparison NPC topology. The number of components between the hybrid and NPC topologies is shown in table 1. The leg's inverter can be connected to points 4, 3, 2, 1 and 0 of the DC-link. A DC/DC converter is used to control the capacitor

voltage of the DC-link. The DC/DC converter is compose by two unidirectional switches, one diode and one coupled inductor. The principles of operation and of the modulation techniques employed are explained in the following.

Table 1. Number of the components.

Topology	IGBT	Diode	Total
NPC	8	6	14
Diode-Clamped	8	4	12

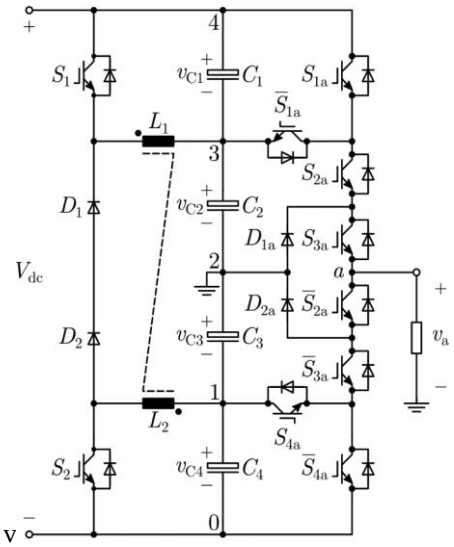


Figure 2. Proposed Five-Level Dioode-Clamped Inverter with DC-Link voltage balancing circuit.

2.1 Operation Mode and PWM strategy of Five-Level Inverter

Table 2 shows the switching states of the converter (for hybrid and NPC inverter) and its respectives output voltages. The switching state 1 is the leg connection at point ('4') of the DC-link. While the switching states 2, 3, 4 and 5 are the leg connection at points ('3'), ('2'), ('1') and ('0') of the DC-link, respectively, as shown in Fig. 3.

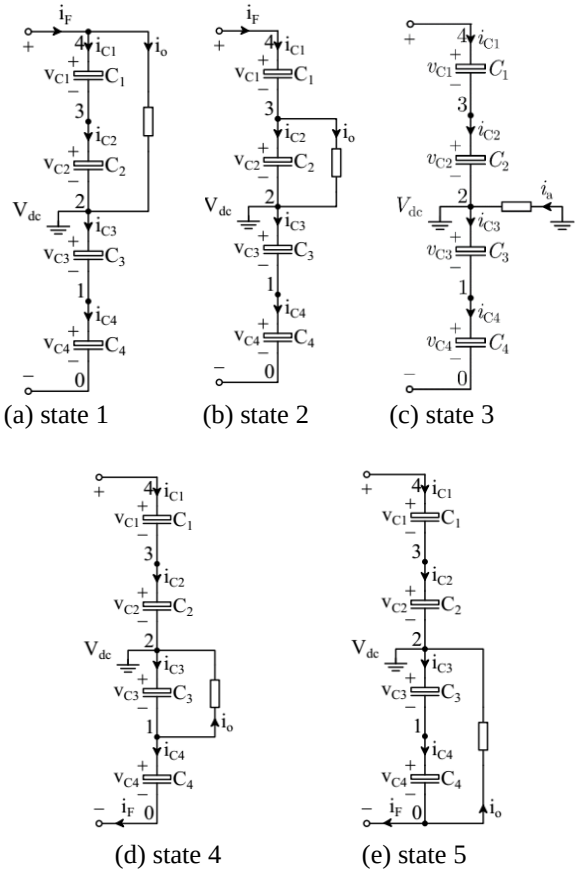
Table 2. States of the switches and output voltage.

state	S1	S2	S3	S4	V_{ao}
1	1	1	1	1	$V_{DC}/2$
2	0	1	1	1	$V_{DC}/4$
3	0	0	1	1	0
4	0	0	0	1	$-V_{DC}/4$
5	0	0	0	0	$-V_{DC}/2$

The LS-PWM modulation is used to operate hybrid inverters and the five-level NPC. It is possible to change the NPC inverter through diode-clamped inverter without change the modulation.

2.2 Capacitor Voltage Unbalanced

It is well known that the neutral point currents of the NPC inverter multilevel can cause unbalances on the DC-link voltages (Rojas et al., 2014; Wang, Li, Zheng, Xu and Fan, 2015; Zeng et al., 2013), and also introduce harmonic distortion in the converter output voltage reducing the its total performance. In Fig. 3 are shown all the configurations for each switching state. Applying the Kirchhoff Law of the currents at the points ('4'), ('3'), ('2') and ('1') it is possible to establish the relationships between the currents of the capacitors to the current that are injected at the intermediate points of the DC-link. In table 3 are presented these relations. Note that inside the switching period the currents of the external capacitors (C4 and C1) are the same as the currents of the internal capacitors (C2 and C3).



(a) state 1 (b) state 2 (c) state 3

(d) state 4 (e) state 5

Figure 3. Switching state

Table 3. Current's relation.

State	Node	Current
1	4	$I_{C4} = i_F + i_o$
2	3	$I_{C3} = i_F - i_o$
4	1	$I_{C2} = i_F - i_o$
5	0	$I_{C1} = i_F + i_o$

Considering that $C_1 = C_2 = C_3 = C_4 = C$, the capacitors voltages can be written as follows:

$$V_{C4} = V_{C1} = \frac{1}{C}\int (i_F + i_o)dt \quad (1)$$

$$V_{C3} = V_{C2} = \frac{1}{C}\int (i_F - i_o)dt \quad (2)$$

Where i_F and i_o are the source and load current respectively. Note that for eq. (1) the external voltages will increase while the internal voltages, see eq. (2), will decrease. In Fig. 4 are presented the simulations for the open-loop hybrid inverter. It is possible to see that the eq. (1) is satisfied. Assuming that V_{C1} +V_{C4} = Vext, V_{C2} + V_{C3} = Vint and that V_{DC} = V_{C1} + V_{C2} + V_{C3} + V_{C4}, the DC-link voltage can be written as follows:

$$V_{DC} = V_{ext} + V_{int} \quad (3)$$

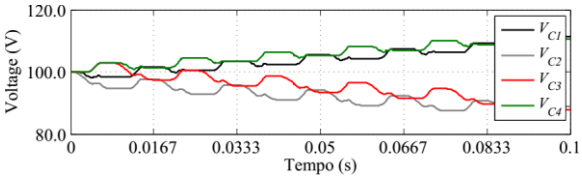
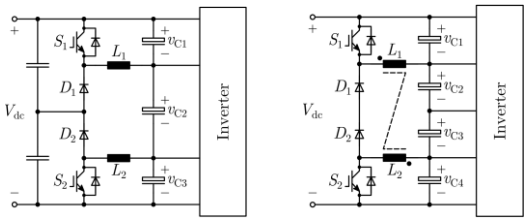


Figure 4. Capacitor's voltage in open loop

3 DC-Link Voltage Control

The DC-link control is perform by the DC/DC converter showed at (Corzine and Majeetha, 1999) as show by Fig. 5(a). In order to decrease the value of the inductances L1 and L2, this work proposes to use a coupled inductor, as shown in Fig. 5(b).



(a) (b)

Figure 5. DC-Link voltage balancing circuit. (a) Four level DC-DC developed by Corzine. (b) Proposed circuit.

The DC/DC converter is based on the Buck Converter operation principle, where V_{int} is given by:

$$V_{int} = dV_{DC} \quad (4)$$

where *d* is the duty-cycle of switches S_1 and S_2. In the Fig. 6 it is shown the control scheme for the DC/DC converter. The voltage error is controlled by a PI controller. The voltage V_{int} its adjuted for $V_{DC}/2$, then:

$$V_{int} = \frac{V_{DC}}{2} = V_{C2} + V_{C3} \quad (5)$$

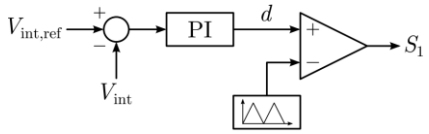


Figure 6. DC-Link control.

Replacing the eq. (5) in eq. (3):

$$V_{ext} = \frac{V_{DC}}{2} = V_{C1} + V_{C4} \quad (6)$$

Replacing the equations (5) and (6) on equation (1):

$$V_{C1} = V_{C2} = V_{C3} = V_{C4} = \frac{V_{DC}}{4} \quad (7)$$

4 Analysis Simulation Results

In order to verify the application of the proposed inverter, the simulation results have been obtained by considering the system in Fig. 2, with the help of MATLAB and PSIM programs. In the Table 4 are presented the simulation parameters.

Table 4. System Parameters Used in the Simulation.

Parameter	Value	Parameter	Value
DC-Link Voltage	4	Carrier Frequency	10kHz
DC-Link Capacitor	3	Load RL	50Ω / 7mH

The DC/DC converter regulates the DC voltage supplied for the inverter and control the capacitors voltages avoiding unbalances through the control of the duty-cycle *d*. The Fig. 7 presents the dc-link capacitor voltage (V_{C1}, V_{C2}, V_{C3} e V_{C4}) in closed loop. Note that the DC-link capacitors voltages are balanced.

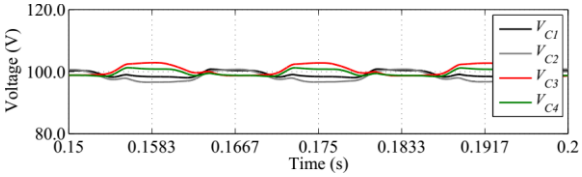


Figure 7. DC-Link capacitor voltages.

Following it is performed the analysis of the hybrid inverter compared to the NPC inverter.

4.1 THD current and WTHD voltage

The Fig. 8 presents the currents i_o and the pole voltage *Vao* of the diode-clamped inverter. The switches have been organized in such a way that the same command signal used in the NPC can be used in the diode-clamped inverter. Replacing the NPC by the diode-clamped inverter does not change the performance over the current THD and WTHD voltage. As show the table 5, the performance difference appears only in the third decimal place of the percentage

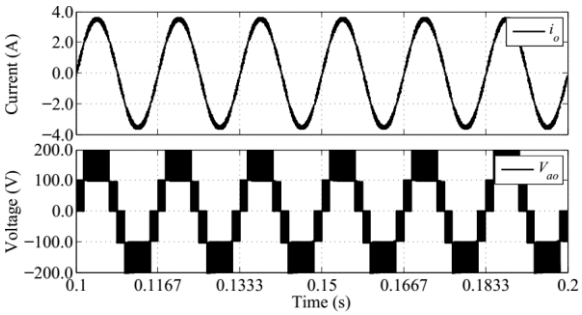


Figure 8. Output signals (current and pole voltage).

Table 5. THD current and WTHD voltage (%).

m	THD		WTHD	
	Diode-Clamped	NPC	Diode-Clamped	NPC
0.5	4.698	4.699	0.304	0.305
0.75	3.831	3.833	0.283	0.283
1.0	2.56	2.560	0.111	0.111

4.2 Condution and Switching Losses

The Fig. 9 shows the diode and IGBT voltages to NPC and diode-clamper inverters.The maximum voltage applied to the four IGBT's of the NPC inverter is 100V (see Figs. 9(b)), while for the diode-clamped topology the IBGT's S1, S2 and S4 the maximum voltage is 100 V, however for IGBT S3 the maximum voltage is 200V (see Fig. 9(a)). The advantage of the diode-clamped topology is in the number of diodes, since it has two diodes less than the NPC topology (see Fig. 9(c)).

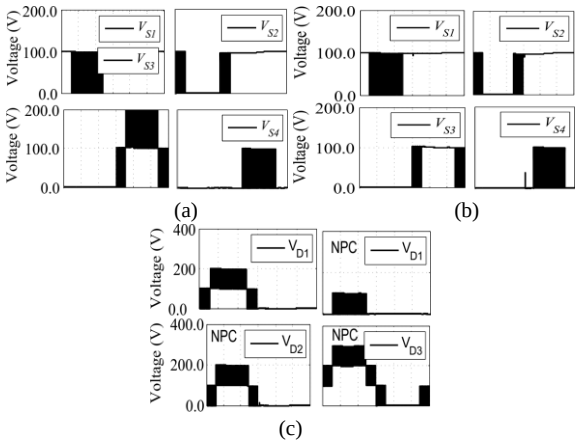


Figure 9. IGBT and diodes voltages. (a) Diode-Clamped (b) NPC (c) Diodes - NPC

The maximum voltage applied to the switches is directly associated with the switching losses. As shows Fig. 10, the NPC topology has 2.07 W of losses, while the diode-clamped topology has 2.65 W. The number of semi-conductors is directly associated with the conduction losses. As the NPC topology has more components the losses are larger.

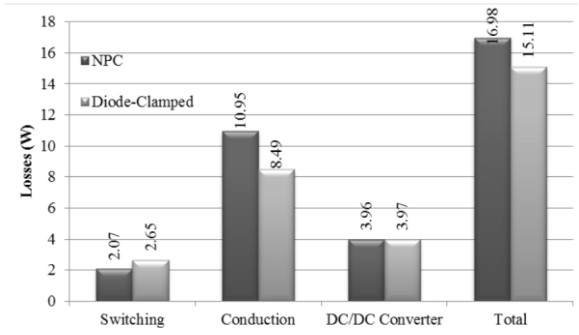


Figure 10. Condution and Switching Losses.

The performance of the DC/DC converter is the same regardless of the topology used. In general, the proposed system with the diode-clamped inverter has a loss of 11%.

5 Conclusion

In this paper, a novel system for diode-clamping multilevel converter with capacitor voltage balancing has been proposed. The proposed system has following features: (i) using a four-level DC/DC converter controlling a 5-level bus with acloped inductors; (ii) Replacement of the NPC inverter by an inverter with a reduced number of components which provided a reduction in losses.

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