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DC-link project applied to Variable Speed Drives in Subsea Power Systems ⋆

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Abstract: This paper presents a project method of the direct current link in order to decouple the rectification and inversion stages present in power electronics converters in a subsea power system, showing the calculation memories of the capacitors to be used in Variable Speed Drives that drive subsea loads. In order to observe the influence of harmonics on the subsea power system and on the voltage of the direct current link, the entire system was modeled with the PSCAD/EMTDC electromagnetic transient software.

Keywords: Retification Stage, Inversion Stage, Resonance, Harmonic Propagation, DC Link, Capacitance, Variable Speed Drives

1. INTRODUCTION

New equipment and marine electrical components have been announced by manufacturers for application in oil extraction in deep waters. In this scenario, the concept of Submarine Power Systems (SPS) arises, in which different types of equipment are used together, such as cables, transformers, electrical machines and power converters, the latter used in variable speed drive (VSD) for subsea motors, in order to perform this complex operation.

The level of detail in the SPS modeling required for this work will certainly subsidize companies to take on the greater challenge of equipment and control system marinization for the most diverse elements used in this activity. This will contribute to the improvement of dc-links projecting in specific applications at ultra deep water operations for the oil industry, in addition to a better understanding of resonance and harmonic propagation problems in umbilical cables. These latter subjects are part of a single set and will be addressed in two other papers that, together with the present paper, are submitted for appreciation by the CBA2020 committee. They are: "Phenomena Analysis of Ferroresonance and Self-Excitation in Subsea Power Systems" and "Comparative Study of Technologies for Harmonic Propagation Mitigation in Subsea Power Systems".

Among all the used equipment, the electric power cable, which connects the platform (topside) to the VSDs located on the seabed, has the highest cost of implementation. Due to the higher inherent capacitance of cables (Akihiro Ametani, 2015), these may have parallel resonances depending on the load being actuated (Merhej and Nichols, 1992), (Liang and Jackson, 2009), increasing the electrical stress on the cable and degrading the Total Harmonic Distortion (THD) of voltages on the topside. Fig. 1 illustrates the SPS model used in this work.

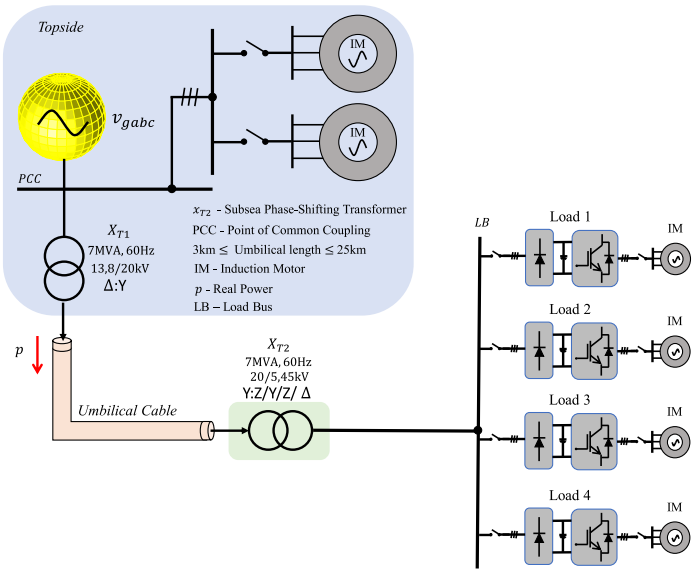

Figure 1. Representation of SPS.

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To reduce costs and complexity of marinization of equipment, a three-phase diode bridge is used for converting alternating current (ac) to direct current (dc), in order to make the interface between the VSD and the underwater engines for oil extraction. The operation of VSDs uses the Sine Pulse Width Modulation (SPWM) strategy. This modulation strategy generates high frequency harmonics in the dc-link current, centered on its switching frequency and its multiples (Mohan et al., 2003). Therefore, it is essential to project the capacitor of the dc-link in such a way that these high frequency harmonics produce a reduced impact on the ac-network, without causing resonances that are not foreseen in the subsea power cable.

This work has the objective of investigating which capacitance value is sufficient to promote the decoupling between the rectification and inversion stages, showing the project of the capacitors to be used in the VSDs that will actuate on subsea loads. The next sections are organized as follows: Section 2 deals with the project methods used to calculate the dc-link's capacitance. Section 3 presents the step-by-step calculation of the dc-link's capacitance value applied to the SPS system (Fig. 1). Section 4 shows the simulation results and how different capacitance values affect the system behavior. Finally, Section 5 depicts the conclusions.

2. PROJECT METHODS

The project and optimization of the used capacitor in the dc-link can be carried out using the following techniques:

- Experimental: Various capacitor values are tested in an experimental way until the closest result to the desired one is obtained. It is a very laborious and costly technique;
- Simulation: It can lead to good results in terms of project but it still requires a lot of time involved in the search process, since each simulation is tested for a specific point of operation that involves a large number of parameters;
- Analytical approach: It presents low cost and commitment in addition to being intuitive. However, for calculations of the capacitor, ripple and losses, approximate formulas (usually empirical) are used.
- Method presented in Hava et al. (2012): Information on topology of the converter, adopted modulation technique and tolerance or not to high voltage ripples help in choosing the type of capacitor (aluminum electrolytic or thin film) and in the iterative process of searching for the optimized capacitance values.

Among the exposed methods, the one presented in Hava et al. (2012) analyzes several operating factors of the system, allowing to take into consideration the type of capacitor that will be used, switching strategy, losses and temperature variation over the capacitor. Therefore, this method was chosen in this work to dimension the dc-link in order to decouple the rectification and inversion stages.

2.1 Characteristic Harmonic Content of the DC-Link's Current

The dc-link of the VSD has current harmonic components from the rectification and inversion stages. The first stage introduces low-order harmonic components due to the three-phase diode rectifier. The voltage waveform produced by this type of rectifier has harmonic components at 6 times the network frequency and at its multiples, the first component being the most dominant. As the impedance of the dc-link is large for these low frequencies, high voltage and current ripples appear.

In the inversion stage, high-order components are introduced, arising from switching at high frequencies. The frequency spectrum of the current demanded by an inverter that uses PWM-modulation has components in the switching frequency, in its multiples and in its side bands. The characteristic of the current ripple depends on the used PWM-method, the modulation index, the magnitude of current supplied to the load and the power factor (Hava et al., 1999), (Un and Hava, 2006), (Ayhan and Hava, 2011).

Depending on the modulation index (m_i) and the power factor angle (ϕ), the same PWM-method can present harmonic concentration at different multiples of the switching frequency (f_c) (Ayhan and Hava, 2011). This fact needs to be considered during the project.

2.2 Spectral Analysis

The spectral analysis of the dc-link current ripple can be performed using the double Fourier series (Zhang et al., 1995), (Bierhoff and Fuchs, 2008), (McGrath and Holmes, 2009), as seen in (1).

$$\begin{aligned} F(x,y) = \frac{A_o}{2} + \sum_{n=1}^{\infty}[A_{on}\cos(ny) + B_{on}\sin(ny)] \\ + \sum_{m=1}^{\infty}[A_{om}\cos(mx) + B_{om}\sin(mx)] \\ + \sum_{m=1}^{\infty}\sum_{n\pm1}^{\pm\infty}[A_{mn}\cos(mx+ny) + B_{mn}\sin(mx+ny)] \end{aligned} \quad (1)$$

The function F(x,y), represented in (1), is obtained after the processing of the current wave and the modulating waves used by the adopted PWM-method. The indices m and n refer to the multiples of the switching frequency and the fundamental frequency (f_0), respectively, so that the harmonics are $mf_c \pm nf_0$.

Then the coefficients A_{mn} and B_{mn} are obtained using the double integral described in (2).

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} F(x,y)\, e^{j(mx+ny)}\, dx\, dy \quad (2)$$

Finally, the current's harmonic components (I_{mn}) can be calculated using (3).

$$I_{mn} = \sqrt{A_{mn}^2 + B_{mn}^2} \quad (3)$$

For project purposes, the consideration of the components of the current ripple is difficult, since it consists of many terms (carrier, its side bands and its multiples), in addition to varying according to the point of operation of the

system. The complexity of the process becomes high, since the loss mechanisms in capacitors are dependent on frequency.

2.3 Equivalent Centered Harmonic Concept

The calculation of capacitor losses can be simplified through the concept of equivalent centered harmonic (Ayhan and Hava, 2011). This condenses the components of the sidebands into the component of the switching frequency (f_s) that originated them. Due to the proximity of these components, the losses in the equivalent series resistance and/or in the dielectric of the capacitors remain approximately the same. The use of this method makes it possible to obtain more precise values of losses than those that would be obtained considering current rms values or a single frequency component. This representation is illustrated in Fig. 2.

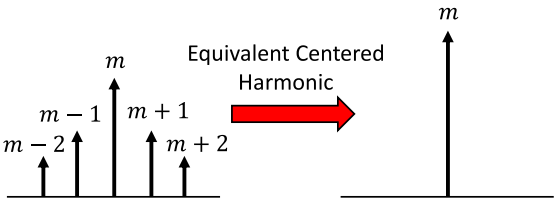

Figure 2. Representation of the equivalent centered harmonic.

The dominant harmonics are found in the first 4 terms of the switching frequency (f_s to $4f_s$) and in their side bands. The exact system can be sufficiently described by considering the first 10 (± 10) components of each of these bands (Ayhan and Hava, 2011). Further in Ayhan and Hava (2011), the authors presented the result of this concept applied to a large number of simulations in order to simplify the processes of choosing the PWM method that produces less harmonic content and the calculation of losses.

Still in Ayhan and Hava (2011), the authors provided in detail the spectral content and dominant frequency components of different pulse width modulation methods, namely: sinusoidal PWM (SPWM), space vector PWM (SVPWM), discontinuous PWM (DPWM1), active zero state PWM (AZSPWM1) and near state PWM (NSPWM), respectively.

In this way, the designer can find which PWM method produces the least harmonic content for his application, as well as estimate component amplitudes without the need to perform the double Fourier transform (1). With these data in place, the calculations of losses and voltage ripple can be performed more easily.

2.4 DC-Link Project Method

Fig. 3 shows the schematic of the bridge rectifier-VSD connection, as well as the harmonic currents in the dc-link. The rms value of the current ripple flowing through the capacitor (I_c) can be calculated as in (4).

$$I_c = \sqrt{I_{ih}^2 + I_{rh}^2} \tag{4}$$

Wherein:

- I_{rh} is the harmonic current from the rectifier;
- I_{ih} is the harmonic current from the inverter.

For rectifiers with diode bridge, the most dominant component of the rectifier current (I_{mD}) can be calculated using (5), having the more dominant frequency equal to 6 times the network frequency (f_s) (Hava et al., 2012).

$$I_{mD} = \frac{P_{load}}{10V_{rms}} \tag{5}$$

Wherein:

- P_{load} is the rated load power;
- V_{rms} is the grid's rms phase voltage;

The calculation of capacitor losses is generally done in an over-estimated manner, using the rms value of the current ripple in the capacitor and the highest equivalent series resistance (ESR). This last parameter depends on the amplitude and frequency of the voltage applied to the capacitor as well as its temperature. The maximum loss ($P_{loss-max}$) can be described by (6).

$$P_{loss-max} = I_c^2 * ESR_{max} \tag{6}$$

Capacitor calculations taking into account (6) result in oversized components. A more detailed analysis can be done through (7), in which the harmonic spectrum of the current and the dependence of the equivalent series resistance with frequency are taken into account.

$$P_{loss} = \sum_{i=1}^{N} (I_{\omega i}^2 * ESR_{\omega i}) \tag{7}$$

Wherein:

- I_ω is the rms value of the dominant component of the harmonic current ripple (Ayhan and Hava, 2011);
- ESR_ω is the equivalent series resistance as a function of frequency.

(7) can be used to calculate ESR losses in both electrolytic and film capacitors, but in the latter type there is an additional portion of losses that occur in the dielectric and that increase with frequency. The inclusion of this portion can be seen in (8).

$$P_{loss} = I_{c-f}^2 * ESR_f + \frac{1}{2} C_{dc} * V_{ripple}^2 * f_{md} * \tan(\delta) \tag{8}$$

Wherein:

- V_{ripple} is the peak-to-peak value of the voltage ripple;
- f_{mD} is the most dominant frequency;
- $\tan(\delta)$ is the dissipation factor, defined as the ratio between the ESR and the capacitive reactance.

The temperature variation (ΔT) in the capacitor is proportional to the dissipated power and the thermal coefficient (R_{th}), as can be seen in (9).

$$\Delta T = P_{loss} * R_{th} \tag{9}$$

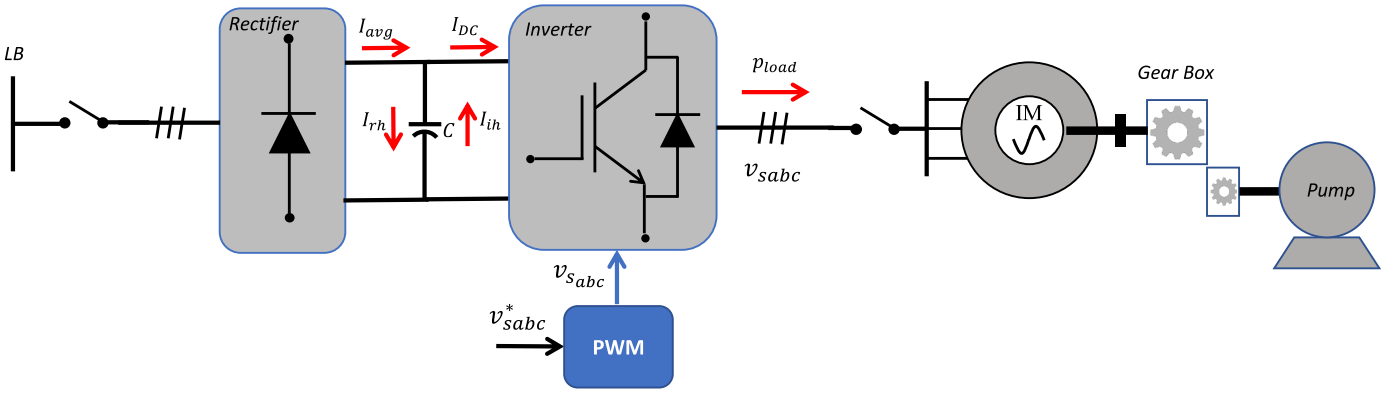

Figure 3. Schematic diagram of one of the 4 subsea loads.

In (8), V_{ripple} can be approximated by the amplitude of the most dominant component of the voltage ripple, being calculated by (10). This requires information on the most dominant component of the current spectrum (I_{mD}), as shown in Ayhan and Hava (2011).

$$V_{ripple} = \frac{1}{2\pi * f_{mD} * C_{dc}} * I_{mD} \tag{10}$$

Finally, the capacitance value can be calculated using (11) (Ayhan and Hava, 2011).

$$C_{dc} = \frac{I_{mD}}{2\pi * f_{mD} * V_{ripple}} \tag{11}$$

3. CASE STUDY

The selection and projecting of the appropriate capacitor type for the target application of this project will be discussed based on the method presented above. Table 1 illustrates the responses for each step in the DC-Link Project.

Table 1. Steps and Answers used in the Flowchart.

Steps	Answers
Converter Topology Selection	2-level VSD with Diode Bridge Rectifier
Modulation Method Selection	SPWM with $f_c = 10\ kHz$
Does DC-Link Have Low Frequency Ripples?	Yes, due to the Rectifier bridge
Is High Voltage Ripple Acceptable?	No

After this procedure, the type of capacitor to be used in the present application was defined to be of the electrolytic type.

The initial estimate of the capacitor value was performed based in (11), using project data such as load rating, voltage and grid frequency. The specification of voltage ripple for decoupling to occur between the rectification and inversion stages was not reported in Hava et al. (2012). The authors only state that values below 1% are acceptable. With only an upper limit, a value for voltage ripple equal to 20 V was settled. This represents 0.27% of the dc-link voltage (V_{dc}), which can be calculated using (12).

$$V_{dc} = 2\sqrt{2} \times V_{rms} = 2\sqrt{2} \times 2610 = 7382\ V \tag{12}$$

In which the value 2610 V in (12) corresponds to the motor's rms phase to ground nominal voltage.

With the value of the voltage of the dc-link, one can, through (5), (10) and (11), calculate the minimum value of the dc-link capacitance, as can be seen in (13).

$$\begin{cases} I_{mD} = \dfrac{P_{load}}{10V_{rms}} = \dfrac{1,24 \times 10^6}{10 \times 2610} = 47,51\ A \\ C_{dc} = \dfrac{I_{mD}}{2\pi f_{mD} V_{ripple}} = \dfrac{47,51}{2\pi \times (6 \times 60) \times 20,00} \\ C_{dc} = 1,1\ mF \end{cases} \tag{13}$$

The normalized harmonic current demanded by the inverter can be estimated, using the spectral content provided in detail in Ayhan and Hava (2011), as $I_ih = 0.6\ pu$. The information was obtained from the normalized 3D-graphic, adopting the SPWM as a modulation method. The chosen operating point considered $M_i = 1.0$ and $\phi = 36°$ (power factor 0.81). This value is normalized by the magnitude of the load's phase current.

The nominal rms value of the VSD's current used in this study is 200 A. In this way, the rms value of the harmonic current demanded by the inverter can be approximated by (14).

$$I_{ih} = 0,6 * 200 = 120\ A \tag{14}$$

Where 200 A corresponds to the rated current of the converter.

Based on the calculated values, (4) is used to combine the effects from the rectification and inversion steps, as can be seen in (15).

$$I_c = \sqrt{47,51^2 + 120^2} = 129,06\ A \tag{15}$$

To investigate the losses in the ESR and the increase in temperature in the element, information from a catalog by the manufacturer Cornell Dubilier Electronics (Dubilier) was used. This catalog features typical ESR curves, normalized by the ESR of 120 Hz @25°C.

Electrolytic capacitors typically have maximum rated voltages around 500 V. Due to the need to associate them in series so that they can be used in a 7.4 kV dc-link and the consequent decrease in the equivalent capacitance, it was decided to choose a higher capacitance, so that the final value remains higher than the projected. For comparative purposes, two capacitors were chosen as candidates for the composition of the dc-link. Its parameters are summarized in the Table 2.

Table 2. Capacitor parameters.

Capacitance (mF)	3.6	11.0
Rated Voltage (V)	450	450
ESR 360 Hz @85 $°C$ ($m\Omega$)	13.7	4.5
ESR 10 kHz @85 $°C$ ($m\Omega$)	11.0	3.6
Rated Current @85 $°C$ (A)	20.2	46.9

The minimum number of capacitors used in the series/parallel arrangement depends on the dc-link voltage and the harmonic current to which they are exposed. The calculation of the loss in each capacitor is performed using (7), being repeated in (16) with the project values and considering the most dominant components of the rectification and inversion.

$$P_{loss} = \left(\frac{I_{mD}}{n_{paralelo}}\right)^2 ESR_{360Hz} + \left(\frac{I_{ih}}{n_{paralelo}}\right)^2 ESR_{10kHz} \quad (16)$$

Where $n_{parallel}$ is the number of serial branches that are associated in parallel.

The temperature variation in each element was estimated using (9) and considering $R_{th} = 3,8\ °C/W$ (Hava et al., 2012). The nominal temperature of the used capacitors is 85 $°C$. Therefore, the sum of the ambient temperature (50 $°C$ (Hava et al., 2012)) with ΔT should not exceed this value. Table 3 gathers information regarding the 2 arrangements made up of 3.6 and 11 mF capacitors.

Table 3. Two studied arrangements.

Capacitance (mF)	3.6	11.0
Series Capacitors	17	17
Branches in Parallel	7	3
Total of Capacitors	119	51
Equivalent Capacitance (mF)	1.5	1.9
Losses (W)	3.9	6.9
Temperature Variation ΔT ($°C$)	14.7	26.2
Element's Temperature ($T_{ambiente} + \Delta T$)	64.7	76.2

As noted in Table 3, both capacitors met the requirements: equivalent capacitance of the arrangements higher than the design (1.1 mF) and temperature of each element below the nominal value (85 $°C$). The arrangement of 11 mF capacitors has the following advantages: higher equivalent capacitance, reduced number of components (51 against 119) and less total loss (352 against 1071 W), although the individual loss is higher. In this way, the project can be considered completed.

4. SIMULATION

In this section, some simulation results are presented in order to apply the theory described to the project in question

Some simulations were carried out in order to illustrate the voltage profiles of the dc-link, the currents from the rectification stage (I_{ret}), inversion stage (I_{inv}), as well as the phase current demanded by the rectifier (I_{aLOAD1}) of one of the 4 subsea loads. The simulated scenarios contemplated capacitance values of 0.5 mF (base case); 1.1 mF (capacitance calculated in section 3); 11 mF and 110 mF.

The variations in the voltage profile of the dc-link can be seen in Fig. 4. As expected, the voltage ripples become smaller and smaller as the capacitance of the link increases.

However, the voltage ripple specified in the project, 20 V peak to peak, was obtained only with a capacitance 10 times higher than that calculated in section 3. The reason for this divergence is due to the used method, since low frequency ripples from the rectification stage, caused by the diode bridge, are only accounted for.

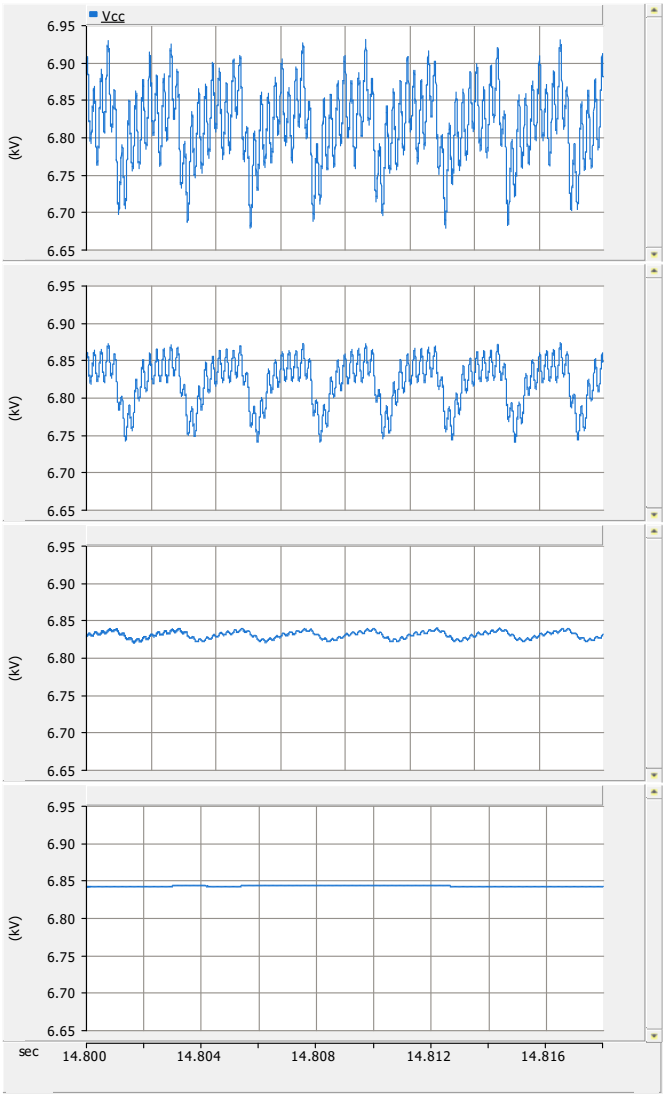

Figure 4. DC-link voltages for capacitance values of 0.5, 1.1, 11 and 110 mF (top to bottom).

To show that such a ripple of I_{inv} originates from the inversion step, the inverter, motor and pump assembly has been isolated from the system and connected to an ideal

dc-voltage source. Fig. 5 shows the current demanded by the inverter after the motor is in steady state.

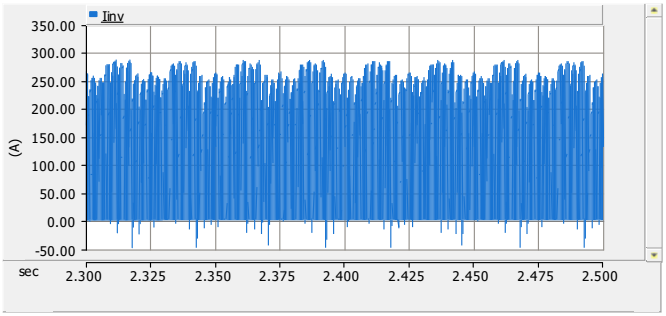

Figure 5. I_{inv} for inverter coupled to ideal dc source.

Fig. 6 shows I_{ret} and I_{inv} for the proposed scenarios, by varying the capacitance. The 1-cycle zoom shown at Fig. 7, shows that the 11 mF capacitance is capable of providing low ripple in the rectifier current.

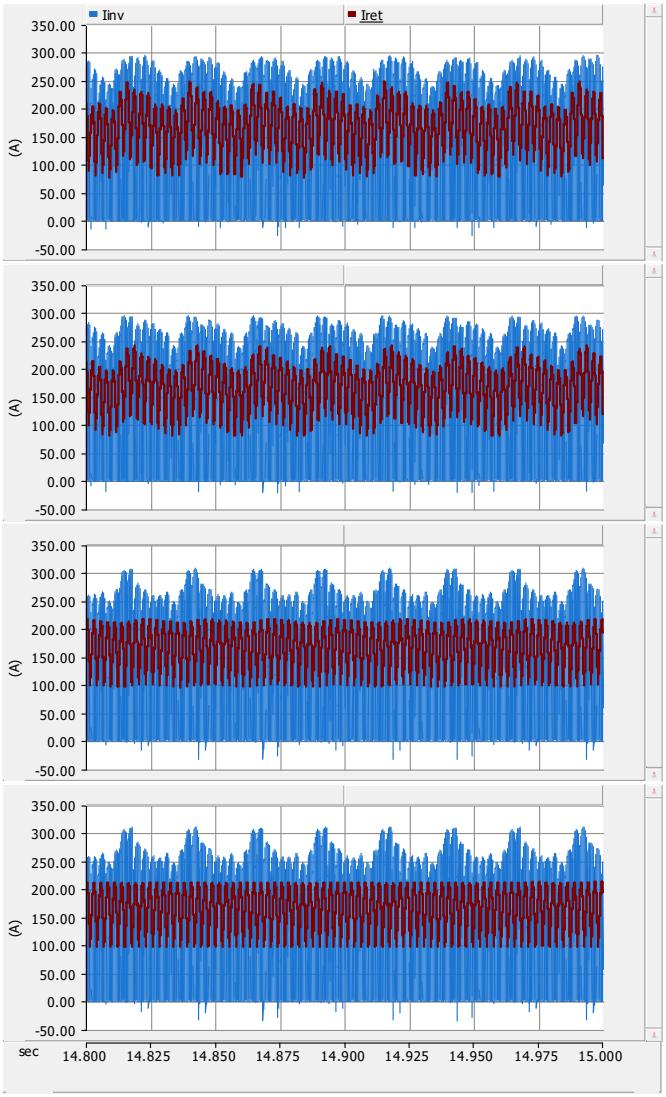

Figure 6. I_{ret} and I_{inv} for capacitance values of 0.5, 1.1, 11 and 110 mF (top to bottom).

The current of phase a of load 1, demanded by the rectifier, can be seen in Fig. 8.

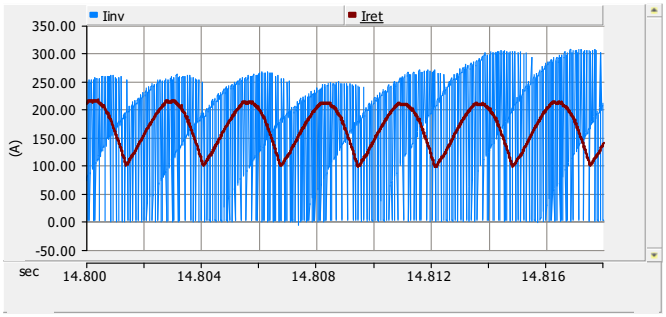

Figure 7. 1-cycle zoom of I_{ret} and I_{inv} for capacitance value of 11 mF.

The total harmonic distortion (THD) of I_{aLOAD1} can be compared for different capacitance values in Fig. 9. As expected, the oscillations become smaller for higher capacitance values.

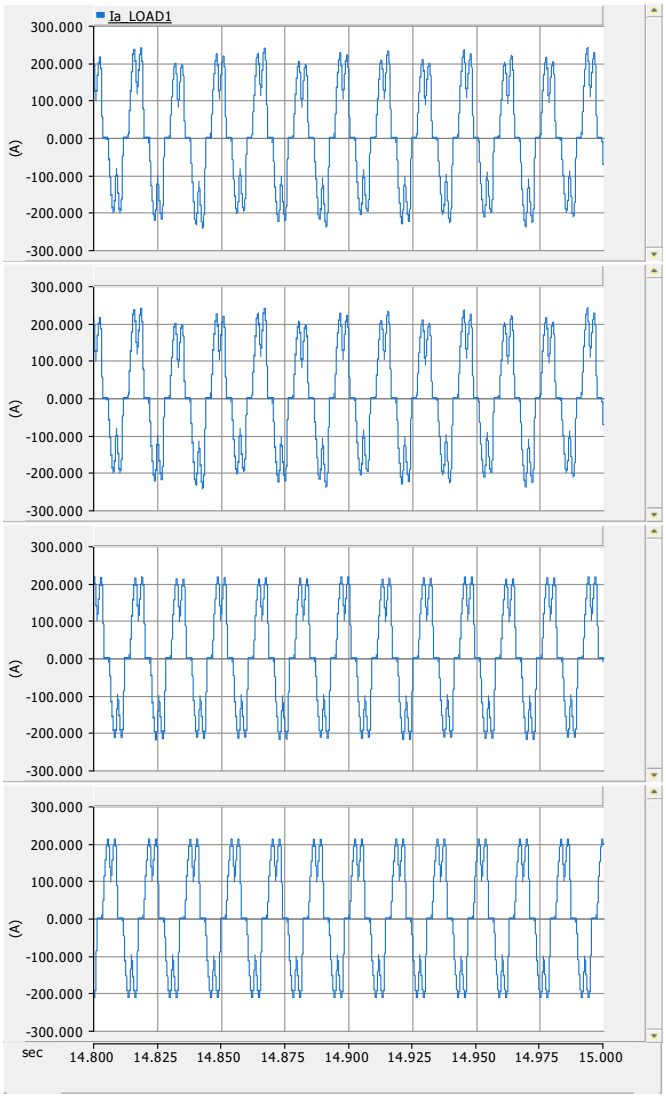

Figure 8. I_{aLOAD1} for capacitance values of 0.5, 1.1, 11 and 110 mF (top to bottom).

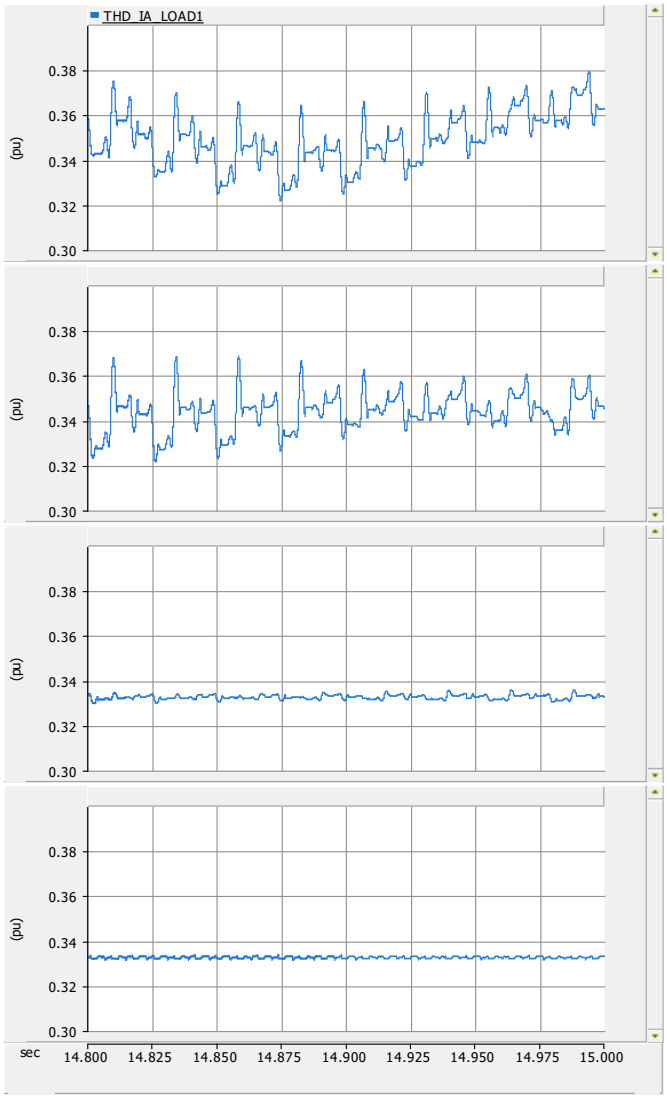

Figure 9. THD of I_{aLOAD1} for capacitance values of 0,5; 1,1; 11 and 110 mF (top to bottom).

5. CONCLUSION

The dc-link project method was described and applied to the project in question, finally indicating the capacitance to be used (1.1 mF). However, for decoupling purposes between the inversion and rectification stages, it was found that the capacitance should be at least ten times higher (11 mF).

The method presented in Hava et al. (2012) considers that the harmonic content generated by the inverter step would be concentrated mainly at high frequencies, being therefore easily filtered by the capacitance present in the dc-link. In this way, the initial estimate of the necessary capacitance is defined by the most dominant component of the current demanded by the rectification step, by its frequency and by the voltage ripple specification of the dc-link. Parameters that are independent of the inverter stage. The most dominant component of the inversion step would only be used in the iterative step of calculating thermal stress and power dissipation. However, these steps were not considered in the dc-link project, due to ideal capacitors used in the simulation.

The calculations of thermal losses and temperature increase in the element were performed based on a capacitor catalog from the manufacturer Cornell Dubilier Electronics (Dubilier). To illustrate the process, series/parallel capacitor arrangements were made in order to make them compatible with the voltages and currents required in the SPS project. Used room temperature and R_{th}, 50 $°C$ and 3.8 $°C/W$, respectively, were chosen arbitrarily to illustrate the calculation process of the described method. Therefore, they must be adapted to the reality of the subsea chamber environment and the used capacitor.

The power dissipated in the 3.6 and 11 mF capacitor arrays can be decreased by adding branches in parallel. In the performed calculations, minimum component numbers were considered so that the rated voltage and current conditions were met.

The harmonic content of the current demanded by the rectifier is concentrated in low orders, even for the smallest simulated capacitance (0.5 mF). The harmonic cancellation provided by the 24-pulse phase-shifting transformer will contribute to increase the quality of the current required by subsea loads. In view of the above, it was verified that it is possible to decouple the inverter and rectifier through the appropriate project of the dc-link. It is clear, therefore, that the dc-link capacitor was able to provide a low impedance path for current ripples in addition to providing damping for voltage ripples from the rectification and inversion steps.

REFERENCES

Akihiro Ametani, Teruo Ohno, N.N. (2015). *CABLE SYSTEM TRANSIENTS Theory, Modeling and Simulation.* John wiley & sons.

Ayhan, U. and Hava, A.M. (2011). Analysis and characterization of dc bus ripple current of two-level inverters using the equivalent centered harmonic approach. In *2011 IEEE Energy Conversion Congress and Exposition*, 3830–3837. IEEE.

Bierhoff, M.H. and Fuchs, F.W. (2008). Dc-link harmonics of three-phase voltage-source converters influenced by the pulsewidth-modulation strategy—an analysis. *IEEE Transactions on Industrial Electronics*, 55(5), 2085–2092.

Dubilier, C. (). Type 520c 85 c long-life, inverter grade, aluminum ultra-ripple, long-life, inverter grade electrolytic capacitor datasheet. `www.cde.com`. Accessed: 2020-01-12.

Hava, A.M., Ayhan, U., and Aban, V.V. (2012). A dc bus capacitor design method for various inverter applications. In *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 4592–4599. IEEE.

Hava, A.M., Kerkman, R.J., and Lipo, T.A. (1999). Simple analytical and graphical methods for carrier-based pwm-vsi drives. *IEEE transactions on power electronics*, 14(1), 49–61.

Liang, X. and Jackson, W.M. (2009). Influence of subsea cables on offshore power distribution systems. *IEEE Transactions on Industry Applications*, 45(6), 2136–2144.

McGrath, B.P. and Holmes, D.G. (2009). A general analytical method for calculating inverter dc-link current har-

monics. *IEEE Transactions on Industry Applications*, 45(5), 1851–1859.

Merhej, S.J. and Nichols, B. (1992). Harmonic filtering for the offshore industry. In *[1992] Record of Conference Papers Industry Applications Society 39th Annual Petroleum and Chemical Industry Conference*, 111–120.

Mohan, N., Undeland, T.M., and Robbins, W.P. (2003). *Power electronics: converters, applications, and design*. John wiley & sons.

Un, E. and Hava, A.M. (2006). Performance analysis and comparison of reduced common mode voltage pwm and standard pwm techniques for three-phase voltage source inverters. In *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC'06.*, 7–pp. IEEE.

Zhang, H., Wheeler, N., and Grant, D. (1995). Switching harmonics in the dc link current in a pwm ac-dc-ac converter. In *IAS'95. Conference Record of the 1995 IEEE Industry Applications Conference Thirtieth IAS Annual Meeting*, volume 3, 2649–2655. IEEE.