DOI: 10.48011/sbse.v1i1.2297

Performance Comparison of 2L-VSC, 3L-NPC, and 3L-MMC Converter Topologies for Interfacing Grid-Connected Systems

Victor R. F. B. de Souza *, **Luciano S. Barros** **, **Flavio B. Costa** *

* *Federal University of Rio Grande do Norte, RN, (e-mails: vicramoneng@gmail.com, flaviocosta@ect.ufrn.br)*
** *Federal University of Paraíba, PB, (e-mail: lsalesbarros@ci.ufpb.br)*

Abstract: Nowadays, power converters play a fundamental role in the conditioning and processing of active and reactive power, and are directly related to power quality indexes. In this sense, new multi-level converter topologies have been integrated in order to provide higher power processing capacity with lower harmonic distortion, switch stress, heating, and losses. The use of these structures compared to conventional two-level converters is especially suitable for high power of the order of megawatt. Considering the relevance of this approach, this paper presents a comparative performance analysis among the conventional two-level topology (2L-VSC) and two multilevel topologies in a grid-connected system: neutral point clamped (NPC) and modular multilevel converter (MMC). Simulation test results present the impacts on voltages and currents for the switches and the whole system, as well as the evaluation of the total harmonic distortion (THD) in order to highlight the crucial points of each topology for this kind of application.

Keywords: performance comparison; two-level voltage source converter; three-level neutral point clamped; three-level modular multilevel converter.

1. INTRODUCTION

The technological advances in power converters have leaded to a high penetration of renewable energy sources (RES) in the power grid. Power electronics devices essentially have the function of interfacing this kind of generation to the power grid, (Bollen and Hassan, 2011; Infield and Freris, 2020). Converters allow the control of currents and voltages in order to adjust the active and reactive power, the direction of power flow, the harmonic distortion levels, as well as aggregate specific functions such as reactive compensation, (Arrillaga and Watson, 2004; Séguier and Labrique, 2012). Usually, the most applications use the conventional two-level converter topology, mainly for simplicity of implementation, lower costs, and less complex control, (Abu-Rub et al., 2014). However, due to technical limitations and the pursuit for larger efficiency, there is a growing search for more sophisticated topologies that provide robustness, power processing capability, and lower levels of harmonic distortion, (Gupta and Bhatnagar, 2017; Dugan et al., 2012). In this sense, multilevel converters have a structure that allow a better distribution of voltages in switches and with the ability to synthesize more sine-shaped voltages, (Abu-Rub et al., 2014; Gupta and Bhatnagar, 2017).

The most discussed multilevel topologies are NPC, (Nabae et al., 1981), flying capacitors (FC), (Meynard and Foch, 1992) and cascade bridges (CHB), (Mcmurray, 1971). The NPC-based topology uses clamped diodes to fix voltage levels per converter arm with the central point of the DC bus connected to the diodes. The FC-based topology has a similar structure to the NPC, but employs floating capacitors instead of diodes to fix the voltage levels. The cascade bridges use half bridge or full bridge association, forming cells where the voltage level is given by the sum of cells. Over the past 15 years with continuous improvements, a topology that has been widely used is the MMC, (Lesnicar and Marquardt, 2003). This structure uses full bridges or half bridges to form series connected submodules, which allows larger flexibility over other topologies. The difference between MMC and CHB is that in the CHB the capacitor voltage depends on the voltage level to be synthesized. Nevertheless, voltage and the connection time in capacitors of the MMC are theoretically equal regardless of the synthetized voltage level, (Du et al., 2017).

Currently, there is a real concern with the impacts of the use of various power converter topologies in several applications. In Lachichi et al. (2019), a performance comparison is performed between a multiport 9 level MMC and a 2L-VSC when associated with a grid-connected AC filter, in terms of efficiency and power in a low voltage hybrid microgrid. The results show that the use of MMC compared to 2L-VSC enables an increase in efficiency as well as a significant reduction in size of the filter.

Salem et al. (2014) presented the effect of different converter topologies on the loss of non-oriented electric steel, comparing two, three, and five level converters. There is a large increase in iron losses for the two-level converter for low frequency carrier and, conversely, the use of multilevel converter presented negligible increases in iron losses. Therefore, this study demonstrated that the use of multilevel structures may be useful for losses reduction that involve the interfacing of power converters in electrical machines.

Singh et al. (2004) presented a review of three phase converters for power quality improvement considering the power factor correction capacity and harmonic reduction. The control for various converter configurations was considered in different applications. The objective was to compare each structure to highlight the suitable choice for each application considering also costs, efficiency, and reliability. The presented results clearly present the superiority of multilevel structures. Vijeh et al. (2019) presented a review with the structural point of view of the main multilevel topologies, in which a detailed comparative study was carried out between topologies and their basic formation cells, presenting a perspective on the number of components, regenerative capacity, and possible combinations based on their basic structure. The review highlights the great flexibility and training capacity of several multilevel structures from the basic structural cell of the presented converters.

Some comparative approaches involving power converters for applications in photovoltaic systems and wind energy conversion systems are also developed in Delavari et al. (2016) and Melicio et al. (2008), respectively. In Delavari et al. (2016), a comparison is made between six multilevel topologies for high power photovoltaic systems focusing on reducing harmonic distortion and improving efficiency. Multilevel topologies present better performance and cost benefits than conventional topologies in medium and high power applications. Melicio et al. (2008) presented a comparison between 2L-VSC and 3L-NPC converters, showing the behavior of the power, currents and output voltages of the converters in a wind energy conversion system using a permanent magnet synchronous generator (PMSG). The NPC converter presented a system performance improvement.

Mademlis et al. (2018) presented a comparative analysis considering iron losses and torque oscillations for a PMSG using 2L-VSC, 3L-NPC and 5L-NPC back-to-back converters, the results demonstrated the improvement of the THD of stator currents and voltages, which affect the iron losses and ripple torque of the generator. In addition, losses are considerably minimized with the use of 5L-NPC. Choudhury et al. (2018) compared the performance of 5L-NPC and 5L-CHB converters in terms of harmonic content reduction, highlighting advantages and disadvantages of each topology. The 5L-NPC presented the best performance.

Based on the above mentioned approaches, the comparison of different converter topologies is important to demonstrate de THD reduction, voltage distribution, robustness, and the structural scalability for each individual converter. Therefore, this paper deals with the performance analysis of three converter topologies, which are 2L-VSC, 3L-NPC and 3L-MMC, for interfacing grid-connected systems in order to verify the impacts on the currents, converter switches voltages, and the reduction of harmonic distortion, discussing the structural aspects as well as the advantages and disadvantages of the three topologies studied.

This work is divided as follows: section II presents the three used converter topologies and the PWM technique employed; section III presents details of the implemented system; section IV presents the obtained results; and section V presents the conclusions.

2. IMPLEMENTED CONVERTER TOPOLOGIES

Three converter topologies (2L-VSC, 3L-NPC, and 3L-MMC) were implemented, and the performance of each one was evaluated considering the THD_i level and the behaviour of voltages and currents in the converter switches.

Fig. 1 depicts the conventional 2L-VSC structure, which can synthesize only two output levels for the pole voltages V_{AO}, V_{BO} and V_{CO}: V_{bus} and 0. However, the phase voltages V_{AN}, V_{BN}, and V_{CN} assume five voltage levels: $\frac{-2V_{bus}}{3}$, $\frac{-V_{bus}}{3}$, 0, $\frac{V_{bus}}{3}$, and $\frac{2V_{bus}}{3}$.

Fig. 2 depicts the 3L-NPC topology, which can synthesize three pole voltages levels: 0, $\frac{V_{bus}}{2}$, and V_{bus}. The phase voltages assume nine voltage levels: $\frac{-4V_{bus}}{6}$, $\frac{-3V_{bus}}{6}$, $\frac{-2V_{bus}}{6}$, $\frac{-V_{bus}}{6}$, 0, $\frac{V_{bus}}{6}$, $\frac{2V_{bus}}{6}$, $\frac{3V_{bus}}{6}$, and $\frac{4V_{bus}}{6}$.

Fig. 3 depicts the 3L-MMC, which has the same three levels of pole voltages and nine levels of phase voltages. Abu-Rub et al. (2014) present the possible switching combinations with their respective output voltages.

The MMC topology presented in Fig. 3 presents a different characteristic for the synthesis of its output voltages due to its modular structure composed by series association of half bridge submodules. Thus, a switching function is determined to establish voltage levels according to the state of switches and, consequently, the capacitors in the submodules, thus:

- If S1 = 1 and S2 = 0, $V_{out} = V_{cap}$;
- If S1 = 0 and S2 = 1, $V_{out} = 0$;
- Else $V_{out} = 0$.

The capacitor average voltage of each submodule is given by:

$$V_{cap} = \frac{V_{bus}}{N_{SM}}, \tag{1}$$

where N_{SM} is the number of submodules per arm of the converter and the number of output voltage levels is given by $N_{SM} + 1$. The number of MMC submodules is two.

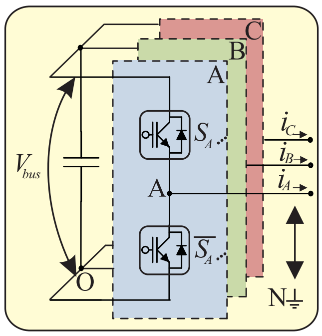

Figure 1. Three-phase 2L-VSC topology.

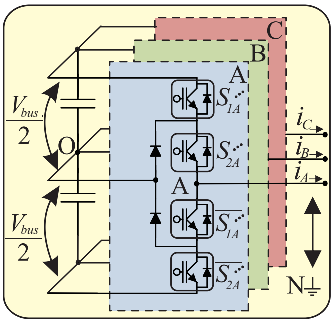

Figure 2. Three-phase 3L-NPC topology.

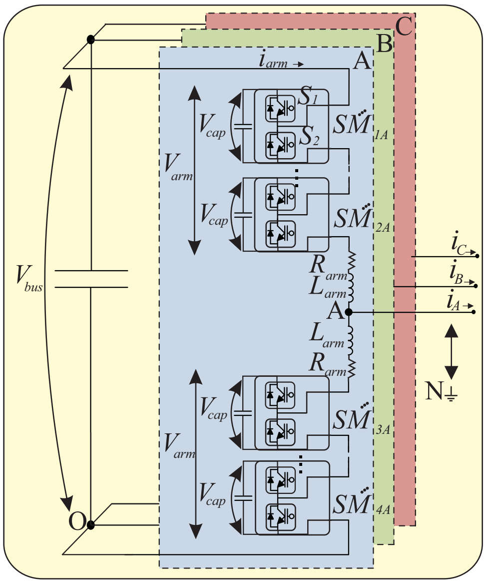

Figure 3. Three-phase 3L-MMC topology.

In the MMC topology, each arm is equivalent to a controlled voltage source V_{arm} with a magnitude given by:

$$V_{arm} = \frac{SM_{active} V_{bus}}{N}, \qquad (2)$$

where SM_{active} is the number of active submodules. Considering V_{SM} the submodule voltage which is the capacitor voltage, the converter arm voltage is a function of the number of submodules, inductance, and resistance arm as follows:

$$V_{arm} = \sum_{n=0}^{n} V_{SM} + L_{arm} \frac{di_{arm}}{dt} + R_{arm} i_{arm}. \qquad (3)$$

Thus, the voltage levels of the MMC are set according to the sum of the submodule voltage in the arm. Moreover, a classification algorithm is used for the voltage balancing. The algorithm employed in this paper is described in Du et al. (2017).

2.1 Employed PWM Technique

The PWM technique used for the implementation of the converters was based on the number of levels of each topology. For the 2L-VSC converter, the Sinusoidal Pulse Width Modulation (SPWM) technique was used, where a triangular carrier is compared to the sine wave modulator for the switch pulses generator, (Holmes et al., 2003).

Regarding the 3L-NPC and 3L-MMC multilevel topologies, the Phase Disposition Pulse Width Modulation (PDPWM) technique was used, which is also based on triangular carrier, but with the number of carriers N_{tri} defined by N-1, where N is the number of converter levels. In this modulation scheme the carriers are shifted in level, have the same amplitude, and are in phase with each other, (Peddapelli, 2016).

3. IMPLEMENTED SYSTEM

Fig. 4 depicts the implemented system consisting of a converter that interfaces a generating source that is represented by a fixed voltage source. The three-phase grid is represented by an infinite bus with a line impedance. Furthermore, the used control is based on the synchronous reference system *dq0*, which performs the converter control through direct and quadrature axis currents in order to properly switch it, imposing output voltages at the terminals, (Abu-Rub et al., 2014).

The described system was implemented in a simulation environment using the Matlab/Simulink platform. The three converter topologies considered SPWM and PDPWM modulation techniques, and the same control structure was considered in all these three converter topologies. In this fashion, the behavior of each topology can be evaluated under the same conditions through currents and voltages, switch blocking voltages, and the THD. Table 1 presents the parameters of the implemented system.

Table 1. System Parameters

Parameter	Value
Grid voltage	311 V
Grid frequency	60 Hz
DC bus voltage	600 V
Switching frequency	5 kHz
Grid line resistance	0.487 Ω
Grid line inductance	42 mH
Capacitor filter	380 uF
Converter filter resistance	0.4 Ω
Converter filter inductance	15 mH

4. SIMULATION AND RESULTS

To analyze the results and observe the system behavior, the point of common coupling voltage (V_{PCC}), converter current (I_{conv}), switch blocking voltage (V_{SW}), switch current (I_{SW}), converter phase voltage (V_{kNconv}) and the total harmonic current distortion (THD_i) were analyzed for each structure, where the index 'k' represents the phase of the converter. The same control structure was employed for all topologies, replacing only the power converters and the modulation technique. The results obtained for the comparative analysis using 2L-VSC, 3L-NPC and 3L-MMC topologies are shown in Fig. 5.

4.1 2L-VSC Topology

For the 2L-VSC topology, the V_{PCC} did not present significant distortions, i.e., it presented a faithful sinusoidal

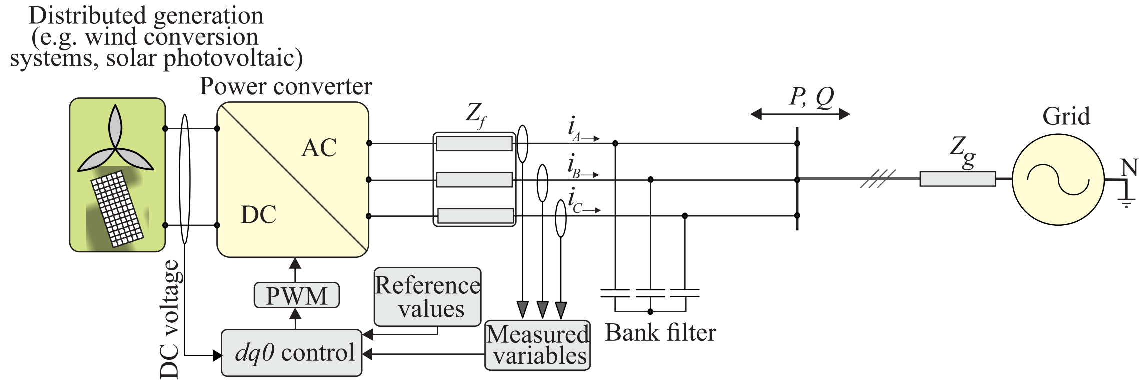

Figure 4. Implemented system diagram.

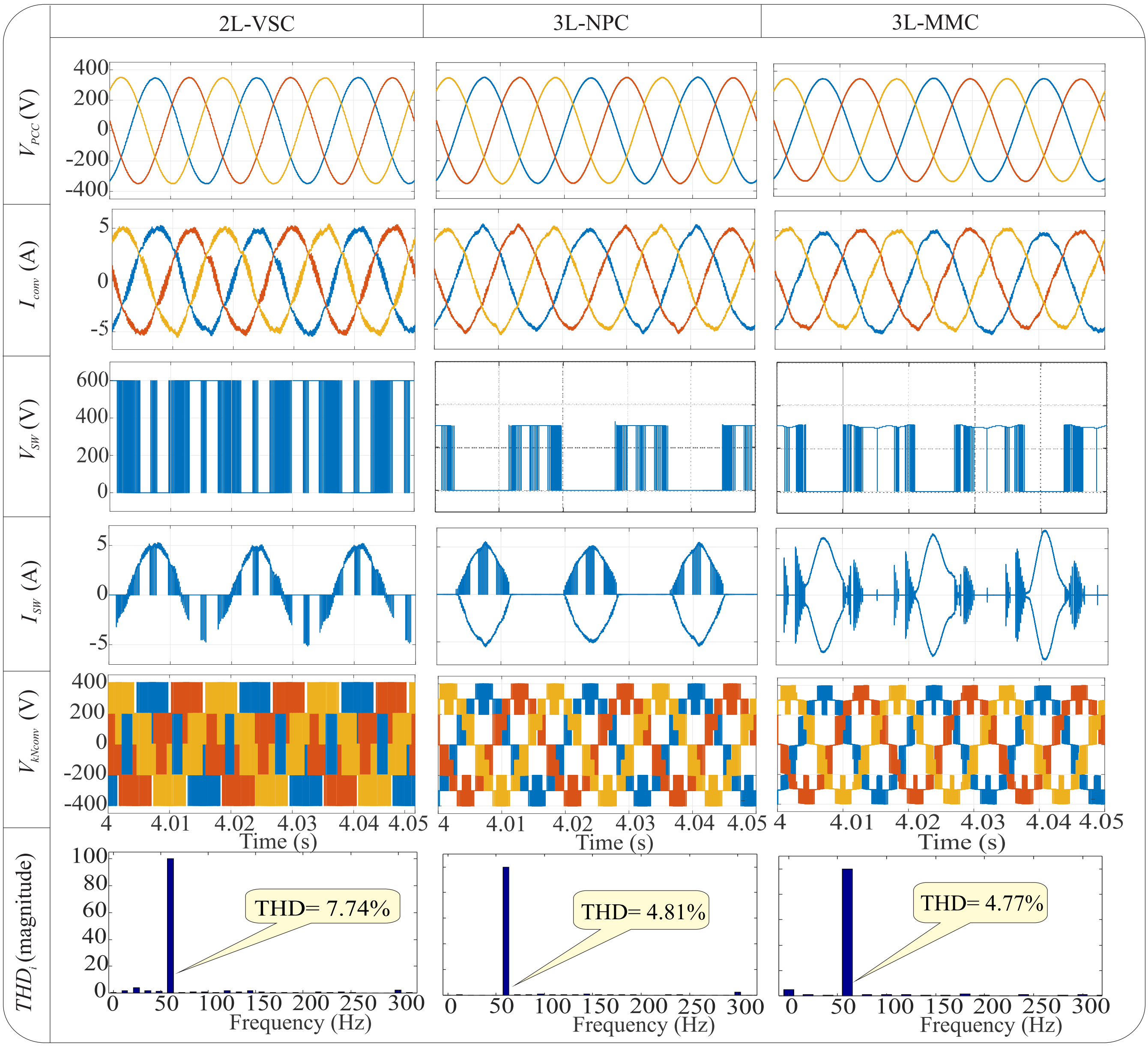

Figure 5. Obtained results for 2L-VSC, 3L-NPC, and 3L-MMC.

shape. However, the currents presented a THD_i of 7.74%, which is directly associated with the low quantity of levels at the converter output. Another particularity of this topology is V_{SW}, which assumed the total value of the

DC bus voltage. The V_{kNconv} obtained for the 2L-VSC correspond to five levels in relation to the DC bus, in this case V_{kNconv} takes this shape due to the switching of the converter. The currents I_{SW} are shown in Fig. 5 and represent the positive and negative semicycle in the converter switches. The positive and negative semicycle of the current in the NPC switches also present lower distortion compared to the 2L-VSC, having this shape due to the commutation periods of the converter.

4.2 3L-NPC Topology

For the 3L-NPC topology, the V_{PCC} did not present considerable distortions. The capacity of synthesize more output voltage levels leaded to an improve in the THD_i, and in this case the currents presented a THD_i of 4.81%. The FFT analysis demonstrated a low THD_i content, which represented a significant reduction of 37.85% in comparison to the 2L-VSC topology. In particular, the voltages of switches and the clamped diodes assumed a half of the DC voltage. This feature gives a technical advantage in relation to the 2L-VSC, with low voltage and thermal stress in the switches. The V_{kNconv} in the 3L-NPC correspond to the nine levels in relation to the DC bus. Therefore, phase voltages are even closer to a sinusoidal shape than in the 2L-VSC. In addition, the current waveforms on the switches for the two semicycles levels are shown.

4.3 3L-MMC Topology

For the 3L-MMC, the V_{PCC} presented the best sine-shaped waveform. In this case, due to its lower THD_i characteristic and the natural arm filtering capacity, this structure provided the best performance with the lowest current distortion with a THD_i of 4.77%, which represents a 38.37% reduction in comparison to the 2L-VSC topology. The blocking voltages of the MMC switches are similar to the NPC topology and assume a half of the DC voltage. Due to having the same number of levels, the V_{kNconv} for the 3L-MMC assume nine levels similarly to the 3L-NPC. In this case, there is a smoother transition during the change of voltage levels. In addition, there were small ripples in the phase voltages. This characteristic is due to the capacitors of the MMC submodules, which is an intrinsic characteristic of this topology, (Du et al., 2017). The currents in the submodule of the MMC switches presents the lowest distortion, and represents the positive and negative semicycles of the current during the capacitor insertion and removal period according to the selection and switching algorithm as described in Du et al. (2017).

4.4 Performance and Comparison of 2L-VSC, 3L-NPC, and 3L-MMC Topologies

Based on the obtained results shown in Fig. 5, there are some particular features for each topology. Initially, although the 2L-VSC topology is less complex in terms of implementation and control, it is limited to a fixed amount of synthesized voltage levels, which causes larger harmonic current distortion.

The 3L-NPC topology can synthesize more voltage levels through the clamping diodes. It has an advantage over the 2L-VSC with lower harmonic current content, better switch voltage distribution and, consequently, lower losses during switching, but presents a higher level of complexity. In some cases it needs to control the voltage of the bus capacitors to minimize voltage unbalances, and with increasing levels the number of diodes increase considerably without expansion flexibility, (Gupta and Bhatnagar, 2017).

The 3L-MMC topology also performed well, adding all the above mentioned advantages of the 3L-NPC topology, without relying on clamping diodes and with a lower harmonic content. However, this topology requires more complex control involving the monitoring balancing algorithm of capacitors voltages. Conversely, from a structural point of view, it has a differential that is its modularity, presenting ease of expansion of the number of levels through the inclusion of submodules, being a very attractive structure for providing redundancy in case of failure of some submodule and for having higher level of robustness, easily fitting into low and high power applications of grid-connected systems, (Lesnicar and Marquardt, 2003). Table 2 summarizes the main differences between the three presented topologies.

Table 2. Comparative summary between conventional VSC, NPC and MMC for any level

Criterion	**VSC**	**NPC**	**MMC**
Clamping diodes	0	$(N\text{-}1)(N\text{-}2)$	0
Number of switches	6	$6(N\text{-}1)$	$12(N\text{-}1)$
Capacitors	DC bus only	$(N\text{-}1)$	$6(N\text{-}1)+1$
Switch blocking voltage	V_{bus}	$\frac{V_{bus}}{(N-1)}$	$\frac{V_{bus}}{(N-1)}$
Modularity	No	No	Yes
Complexity	Low	Medium	High
Voltage balancing	No	DC bus only	Per submodule
Redundancy	No	No	Yes

The increased complexity and costs involved in implementing a multi-level converter topology, with emphasis on MMC, can be easily justified and may be a suitable solution for several applications involving the need for increased power processing, redundancy, low THD and higher efficiency, being attractive to photovoltaic and wind energy conversion systems, allowing for expansiveness through its modular characteristic.

5. CONCLUSIONS

This paper presented the comparison among the 2L-VSC, 3L-NPC and 3L-MMC topologies, highlighting their advantages and limitations under operating conditions using the same control structure. The 2L-VSC topology presented the lowest complexity of implementation and control design. Conversely, it has technical limitations regarding output voltage levels, switch voltages, and higher THD_i. The 3L-NPC presented better THD_i than the 2L-VSC due to higher output voltage levels. However, this topology is not easy to expand to a higher number of levels, besides the drawback of the large number of clamping diodes. The 3L-MMC, which has a more complex structure, presents lower THD_i than the NPC with the same number of levels. The MMC is easy to expand to a larger number of levels due to its modular structure. In addition, the MMC filtering capacity can be enhanced by exploring the arm impedance characteristics. Thus, based on the results, the use of a multilevel structure can synthesize more sine-shaped output voltages, meet harmonic distortion requirements, and reduce stress on the converter switches. It also has a direct impact on the reduction or elimination of filters that present design complexity, reflecting in the reduction of weight and costs for grid-connected systems. As a continuation of this paper, comparisons among the three presented converter topologies using accurate modelling of photovoltaic and wind energy conversion systems will be considered in order to verify the impacts on the performance of these systems.

ACKNOWLEDGMENT

This work was supported by the National Council for Scientific and Technological (CNPq) and by the Coordination for the Improvement of Higher Education Personnel (CAPES), Brazil.

REFERENCES

Abu-Rub, H., Malinowski, M., and Al-Haddad, K. (2014). *Power electronics for renewable energy systems, transportation and industrial applications.* John Wiley & Sons.

Arrillaga, J. and Watson, N. (2004). *Power System Harmonics.* Wiley InterScience electronic collection. Wiley.

Bollen, M.H. and Hassan, F. (2011). *Integration of distributed generation in the power system*, volume 80. John wiley & sons.

Choudhury, S., Nayak, S., Dash, T.P., and Rout, P.K. (2018). A comparative analysis of five level diode clamped and cascaded h-bridge multilevel inverter for harmonics reduction. In *2018 Technologies for Smart-City Energy Security and Power (ICSESP)*, 1–6.

Delavari, A., Kamwa, I., and Zabihinejad, A. (2016). A comparative study of different multilevel converter topologies for high power photovoltaic applications. In *2016 7th Power Electronics and Drive Systems Technologies Conference (PEDSTC)*, 415–420.

Du, S., Dekka, A., Wu, B., and Zargari, N. (2017). *Modular multilevel converters: analysis, control, and applications.* John Wiley & Sons.

Dugan, R., McGranaghan, M., Santoso, S., and Beaty, H. (2012). *Electrical Power Systems Quality, Third Edition.* McGraw-Hill Education.

Gupta, K.K. and Bhatnagar, P. (2017). *Multilevel inverters: conventional and emerging topologies and their control.* Academic Press.

Holmes, D., Lipo, T., and Lipo, T. (2003). *Pulse width modulation for power converters: principles and practice.* IEEE Press series on power engineering. IEEE Press.

Infield, D. and Freris, L. (2020). *Renewable energy in power systems.* John Wiley & Sons.

Lachichi, A., Junyent-Ferre, A., and Green, T.C. (2019). Comparative optimization design of a modular multilevel converter tapping cells and a 2l-vsc for hybrid lv ac/dc microgrids. *IEEE Transactions on Industry Applications*, 55(3), 3228–3240.

Lesnicar, A. and Marquardt, R. (2003). An innovative modular multilevel converter topology suitable for a wide power range. In *2003 IEEE Bologna Power Tech Conference Proceedings,*, volume 3, 6–pp. IEEE.

Mademlis, G., Liu, Y., and Zhao, J. (2018). Comparative study of the torque ripple and iron losses of a permanent magnet synchronous generator driven by multilevel converters. In *2018 XIII International Conference on Electrical Machines (ICEM)*, 1406–1412.

Mcmurray, W. (1971). Fast response stepped-wave switching power converter circuit. US Patent 3,581,212.

Melicio, R., Mendes, V.M.F., and Catalao, J.P.S. (2008). Two-level and multilevel converters for wind energy systems: A comparative study. In *2008 13th International Power Electronics and Motion Control Conference*, 1682–1687.

Meynard, T. and Foch, H. (1992). Multi-level choppers for high voltage applications. *EPE journal*, 2(1), 45–50.

Nabae, A., Takahashi, I., and Akagi, H. (1981). A new neutral-point-clamped pwm inverter. *IEEE Transactions on industry applications*, (5), 518–523.

Peddapelli, S. (2016). *Pulse Width Modulation: Analysis and Performance in Multilevel Inverters.* De Gruyter.

Salem, A., Abdallh, A.A., De Belie, F., Dupré, L., and Melkebeek, J. (2014). A comparative study of the effect of different converter topologies on the iron loss of nonoriented electrical steel. *IEEE Transactions on Magnetics*, 50(11), 1–4.

Séguier, G. and Labrique, F. (2012). *Power electronic converters: DC-AC conversion.* Springer Science & Business Media.

Singh, B., Singh, B.N., Chandra, A., Al-Haddad, K., Pandey, A., and Kothari, D.P. (2004). A review of three-phase improved power quality ac-dc converters. *IEEE Transactions on Industrial Electronics*, 51(3), 641–660.

Vijeh, M., Rezanejad, M., Samadaei, E., and Bertilsson, K. (2019). A general review of multilevel inverters based on main submodules: Structural point of view. *IEEE Transactions on Power Electronics*, 34(10), 9479–9502.