TRENDS ON POWER CONVERSION USING MOS TECHNOLOGIES

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Abstract - The development of power semiconductor devices leaded mainly by Metal-Oxide-Semiconductor (MOS) Technology, brought an intensive evolution to Power Electronics.

The first part of this paper gives a brief review of the new features of power devices and power integrated circuits (PICs), and describes new important functions. The ability of MOS technology to implement the required isolation to merge in the same chip the power device and its control and protection circuitry is stressed.

A review of fundamental tools for computer aided design (CAD) of smart power devices and electronic power conversion circuits using new topologies with resonant switching is presented. Special emphasis is given to modelling power MOS transistors since theirs models are generally not available in general purpose circuit simulators such as the SPICE program. To demonstrate the accuracy of the referred model a simple example of a power converter with its control and protection circuits is presented and compared with experimental data.

1. INTRODUCTION

Power integrated circuits (PICs) are being investigated with the objective of obtaining efficient power conversion and control of high voltages and high currents. The power delivered by the PIC into a load can be from tens to thousands of watts (Rumennik - 1985). Smart Power Devices are PICs which aim to control low voltages and high currents in automotive applications, robotics, aircraft, and motors, and they are receiving most of the researchers interest, at the present time.

A smart power switch operates as an interface between a control system and a power load, and its structure incorporates in the same monolithic circuit the power device and its control and protection functions. For example, a power transistor that drives a motor or a relay and has current limitation, thermal protection, and for which status messages can be sent back to a microprocessor is a smart power device.

When a power device is integrated with a control circuit on a single chip, greater improvements are achieved in performance, at lower costs, than when control circuits and power ICs are packed separately. The savings come from eliminating the many packages to house individual chips, abolishing the interface circuits between power ICs and control ICs, and shrinking the overall system size. Furthermore, the integration of power devices and control ICs enables a range of functions - temperature control, overvoltage and overcurrent protection - which were unavailable or difficult to implement with discrete power devices.

The advantages of MOS technology over bipolar technology have been frequently pointed out over the last decade (Ohr - 1980; Aloisi - 1981):

– the conduction is based on majorities carriers, thus the switching times are small,

– the current temperature coefficient is negative, thus devices can be easily connected in parallel,

– the input static impedance is high, which reduces greatly drive circuits power levels.

Although power MOS technologies are pushing devices to ideality, when they are embedded in power electronic circuits their features present some shortcomings:

– transient overvoltages due to fast turn-off in inductive circuits,

– high R_{DSON} due to the ability to support extremely high voltages (extended epidrain region),

– capacitive switching losses due to internal capacitances related to the ability to handle high current levels (large channel width),

– low input dynamic impedance which requires extremely high dynamic currents to efficiently drive power MOS devices.

There are several ways to overcome these limitations, most of them cumbersome (like snubbers). New approaches are being studied towards a faster, lighter and monolithic solution.

Some important drive and protection functions for MOS devices have already been developed in the last couple of years and have been tested in new products (Reinmuth, Lorenz - 1989); some specially aiming automobile industry are appearing (Tihanyi - 1987; Garve - 1989).

To design efficient drives and protections, the analysis of the loops that perform these functions requires an efficient model for power MOS devices which accurately simulates their switching behavior. Such models are also very useful for the design and optimization of new power conversion topologies which use resonant switches, the behavior of which is determined by the MOS transistor capacitances.

The first part of this paper deals with the ability of MOS technologies to merge in the same chip the power device and circuitry for its control. The isolation problem is reviewed, and functions like efficient drive and protection against overvoltage, overcurrent and overtemperature are described.

The second part of the paper reviews a model which accurately simulates the switching behavior of a VDMOS. The model, implemented on the SPICE program is used to optimize, either the control circuitry of smart power devices, or the power circuit where it is embedded. Experimental results with an overvoltage protected VDMOS transistor are presented.

2. MOS TECHNOLOGY FEATURES

The simplicity of MOS technology permits the merging of power devices and their control in the same chip. These monolithic solutions are highly desirabe not only to reduce the interfaces, and thus the volume and weight, but also to increase the efficiency of control circuits, namely the sensing (temperature, overcurrent, overvoltage) and fast feedback information.

Among all MOS devices the VDMOS is the most widely used for power integrated circuits that control high currents, usually called smart integrated circuits (Smart Power).

The maturity of CMOS technology, its low power drive requirements, its low sensitivity to temperature, and lower supplies voltages, make it particularly well suited to the implementation of the control circuitries for smart power. Tremendous improvements are being made in PICs. Among the major accomplishments are:

– the development of adequate isolation between high-voltage devices and low voltage control circuits

– the design of devices and fabrication processes that lead to both high voltage and high current at an economical level

– the design of high-voltage, high-current devices that can operate as current sources

3. ISOLATION DEVELOPMENTS

The isolation techniques used in PICs are based on highly complex and costly technological solutions:

Self-shielding

This technique (Baliga - 1986) uses the n^- layer both as the PMOS transistors substrate and as the drain of the VDMOS transistor (fig. 1). NMOS transistors and other components are implemented with diffused p wells to achieve isolation.

This isolation is based on the reverse biased pn^- junctions, which present high levels of static isolation, but the capacitances associated with them do not enable proper dynamic isolation. In fact, voltage transients in the substrate n^- may induce on the p regions enough current flow to forward bias n^+p junctions (VDMOS source - NMOS base) producing latch-up.

Junction isolation

This technique (Zembrano - 1987) uses a double epitaxial layer n^- and p over the substrate n^+ and a buried layer n^+ between the surface layer n^- and the substrate n^+ (fig. 2), which enables the current to flow vertically. The p layer acts as the isolation element between control circuitry and the drain.

The p^+ islands provide isolation to all low voltage circuits from the high voltage device (VDMOS); nevertheless, this complex technique (over 12 masks) is not able to avoid the latch-up effect on fast transients.

Dielectric isolation

This technique (Lu et als - 1988) uses crystal silicon islands on a polycristalline substrate separated by a thin oxide SiO_2 layer (fig. 3).

This technique fully avoids reverse currents at high temperature levels, and reduces latch-up very effectively, but it is very expensive and requires non conventional precautions.

On the self-shielding method both the power device and the control circuitry share the same highly resistive substrate, the epilayer. Beneath the high power region, the

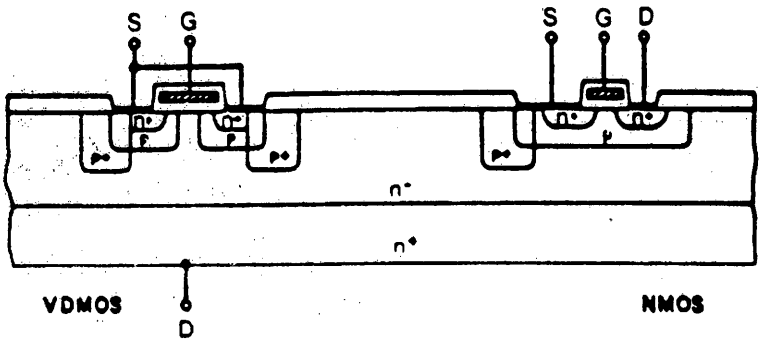

Figura 1. Schematic cross section of a self-shielding vertical structure

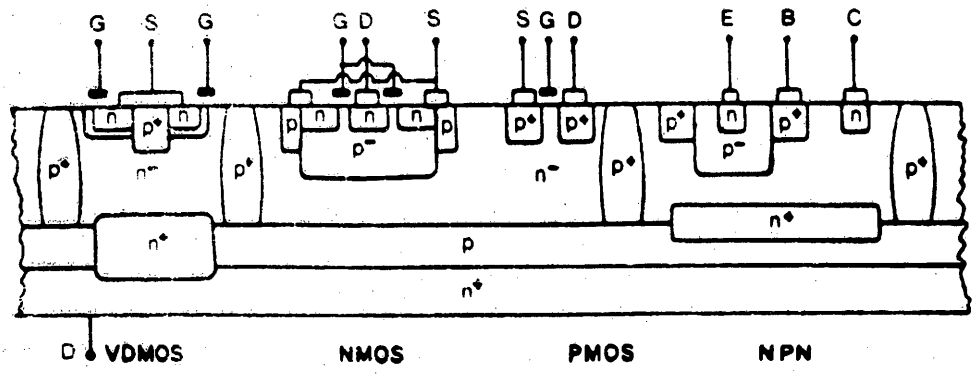

Figura 2. Schematic cross section of a vertical junction-isolation structure

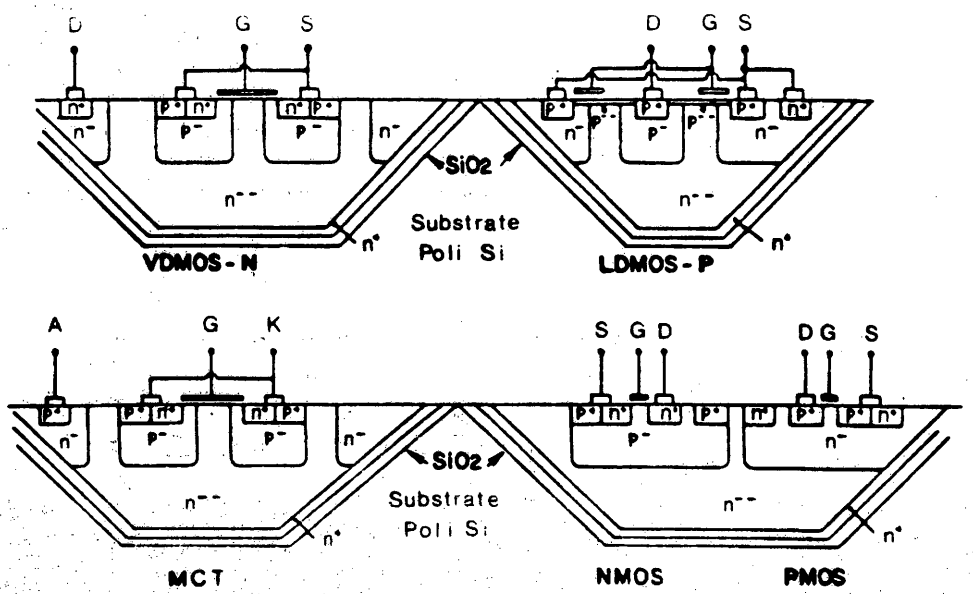

Figura 3. Schematic cross section of a struture using dielectric isolation

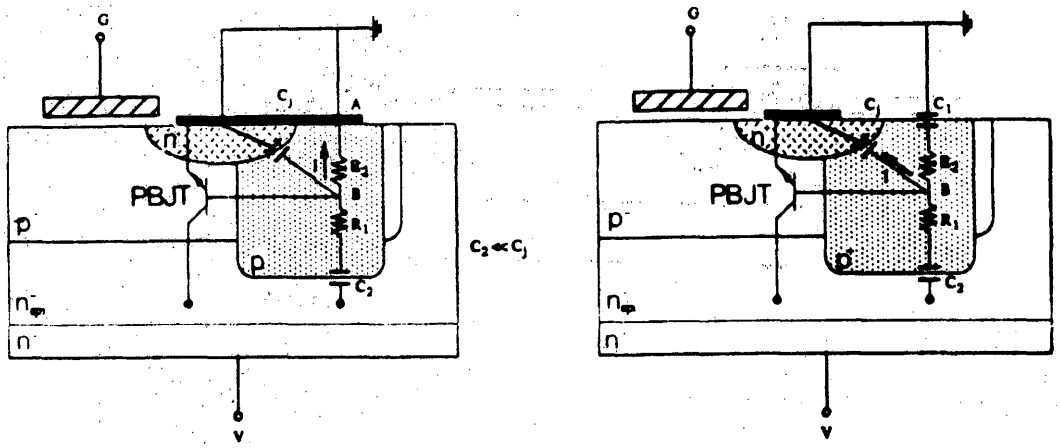

Figura 4. Schematic cross section of a structure a) with the p well grounded, b) with the p well floating.

epilayer is submitted to voltage transients which may induce important current flows into the low power circuit. The voltage drop on the p^+ well, related to these currents can forward bias the n^+p^- source-substrate junction, turning-on the parasitic bipolar transistor, thus reducing the breakdown voltage (fig.1). To avoid this undesirable behavior a new self-shielding method with floating p wells was recently presented (Bafleur et als - 1989) (fig. 4).

This methodology allows, in static behavior, the short diode n^+p^+ to short-circuit the base-emitter junction of the parasitic bipolar transistor. This provides a path for the flow of the reverse currents of the junctions epilayer n^-/p^- and epilayer n^-/p^+ toward the ground through this n^+p^+ diode, without being amplified by the bipolar transistor effect. Thus, the break-down voltage remains almost equal to the theoretical value. Furthermore, in its dynamic behavior the short diode n^+p^+ sinks the parasitic current flow through its high junction capacitance C_j .

4. SMART FUNCTIONS

Introduction

The most important functions performed by the PICs are related to: a) the highly demanding operating conditions of the power device during switching transients, when embedded in power conversion circuits (Simas, Piedade - 1987); b) the increase of efficiency (Simas, Piedade - 1989). Some of these functions are dependent on the switch-load connection. If the switch is implemented by one device, the load can be connected to the source (high-side switch) or to the drain (low-side switch). If the switch is implemented by more than one electronic device, they can be connected in a half bridge or in a full bridge configuration (fig. 5).

The high-side switch configuration occurs specially in automotive applications, to avoid the risk of electrostatic corrosion, but originates driving problems. In fact, to reduce

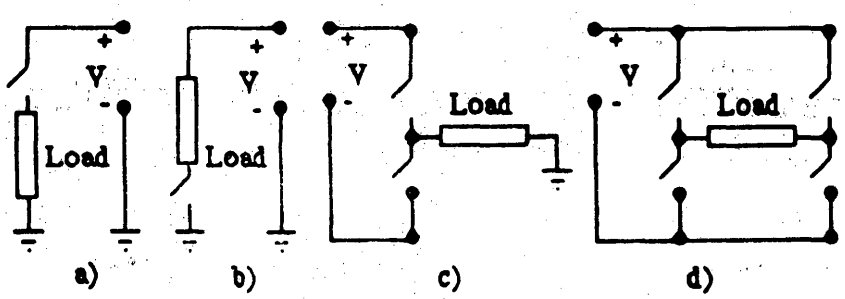

Figura 5. Different switch-load connections in electronic power converters:
a) High-side switch, b) Low-side switch, c) Half bridge, d) Full bridge

the channel ON-resistance, the gate voltage must be at least 6V higher than the drain voltage. The same problem occurs when driving N-channel power MOS devices in bridge circuits. Since electron mobility is about twice the hall mobility, it is less costly to use N-channel MOS devices in spite of the greater difficulty to drive them in bridge configurations.

It is possible to accomplish this form of driving in different ways: a separate gate supply circuit, the voltage of which is higher than the drain voltage; a DC-DC converter; a *bootstrap technique*; or a *charge pump.*

Smart power devices aim to interface a control circuit, for example a microprocessor, and the load. They must be able to act according to signal commands and to protect themselves against *overvoltages*, *overcurrents* and *overtemperatures.* During operation, smart power devices may also produce information about the load state or faulty operation, like the automobile *battery discharge* for instance, through a display with separate voltage power supplies.

Some of these important functions will be described in the following.

Bootstrap technique

An implementation of the bootstrap technique (Young - 1989) (fig. 6) achieves the charge of the bootstrap capacitor through a resistor and a diode during the transistor OFF state. A zener diode limits the floating supply voltage to the value required to enable a fast turn-on of the device.

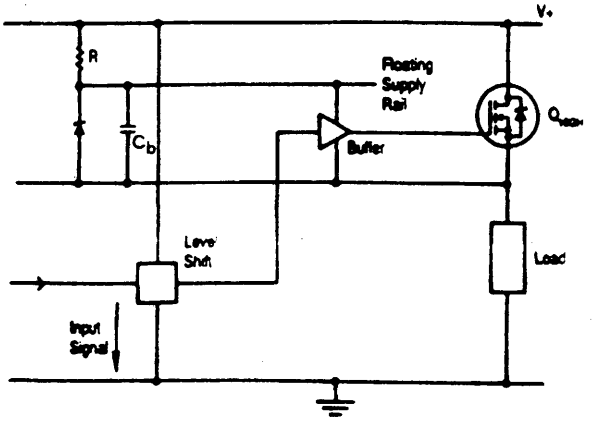

Figura 6. Bootstrap technique.

Charge Pump Circuit

Using the vertical parasitic bipolar transistor of the floating-wells technology, a charge pump circuit was proposed (Elmoznine and als - 1990) (fig. 7). The NPN transistor T1 drives the VDMOS gate, through the current source I_{bias}, until a voltage almost equal to the supply voltage appears across gate-drain. The pipolar transistor T2, switched at the clock frequency, charges the capacitor C_p every negative step. The C_p discharge to the VDMOS gate occurs every positive step, providing a gate voltage step over the supply voltage. Furthermore the bipolar transistor T3, also operating at clock frequency, turns-off the MOS transistor M, thus avoiding the gate discharge through Cp.

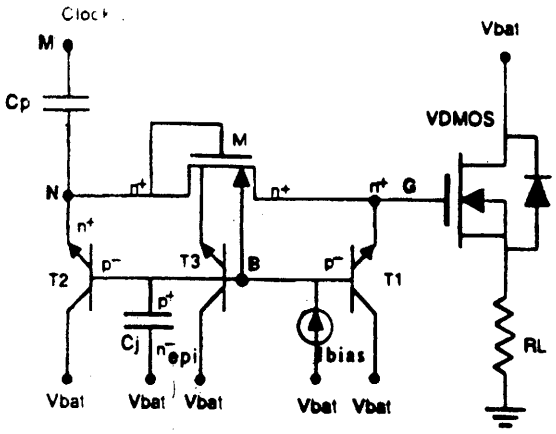

Figura 7. Charge pump technique

Overtemperature Protection

This circuit (fig. 8) is based on the reverse current dependence on temperature (Bafleur et als - 1988). In fact, reverse current has two terms, one related to the diffusion current dependence on n_i^2, and the other related to thermal generation and dependent on n_i (n_i is the carriers intrinsic density). Thus, the diffusion term has an important increase with temperature. This diffusion current variation can be detected on a highly resistive element implemented by means of a NMOS transistor with source and gate short-circuited (fig.8). This acts a Schmidt trigger, with histeresis

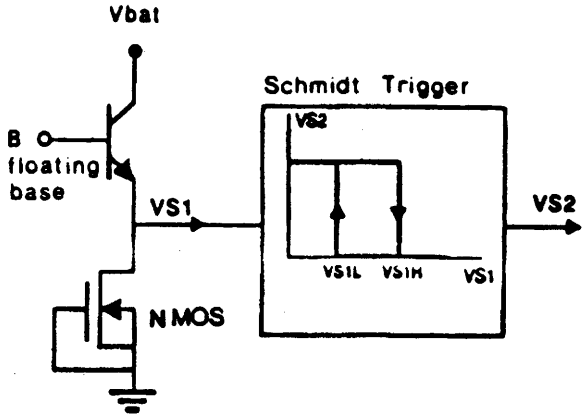

Figura 8. Overtemperature protection circuit

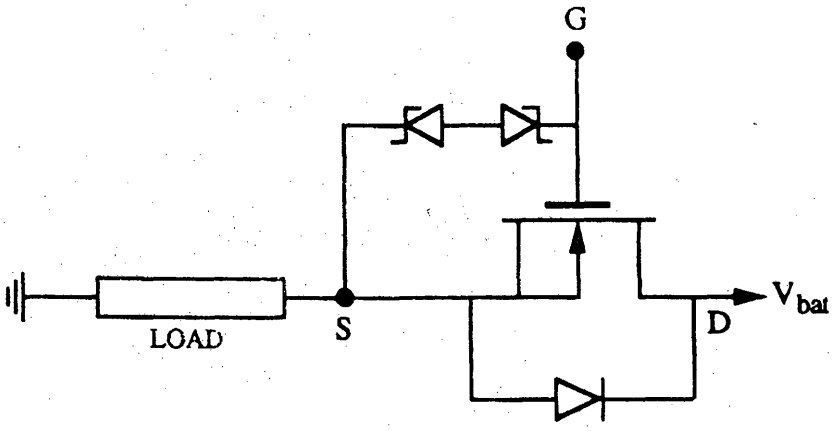

Figura 9. Overcurrent protection circuit.

to avoid oscillation, thus turning-off the power device through the charge pump circuit and sending the fault information to the diagnosis circuit.

Overcurrent Protection

Current sensing is obtained by the isolation of a few cells in the power transistors structure, to provide an accurate fraction of the drain current as a feedback parameter for control and overcurrent protection. However, this approach is not able to distinguish between a true overcurrent fault and the typical overcurrent transient which occurs when driving automobile lamps or motors.

Another solution (Bafleur et als - 1989), which provides a self-limitation of the VDMOS drain current, uses two zener diodes in series between the VDMOS gate and source terminals (fig.9), with a common anode. It is based on the VDMOS saturation current with a low gate-source voltage. In fact, in normal operation, since the gate-source voltage is only 6V, the two zener diodes are off. When a short-circuit occurs, the source voltage reaches zero volts, forcing the zener diodes to conduction, thus limiting gate voltage to 6.6V until the source voltage increases, and keeping the drain current to its maximum value defined by the battery voltage applied to the drain-source and V_{GS}=6.6V. The diode current acts as extra current to the load, which has the advantage of providing both overcurrent protection and enough current to turn-on transients. Nevertheless, it is important to assure the power device turn-off if the short-circuit remains.

This can be accomplished by a circuit that senses the source voltage introducing a delay similar to the current transient time. This calls for an integrator with a high time constant, Highly resistive transistors are prone to the latch-up effect and high capacitances implementation demands large area. The floating p wells principle, referred previously, provides highly resistive transistors avoiding latch-up effect. In fact, the floating p well enables the coupling between substrate and drain by a capacitance (C_2, fig. 4), thus providing negative voltage values in the p^- region which follows the negative drain voltage step. If C_2 is high enough to avoid an increase of more than 0.7V in the drain to substrate voltage, latch-up will never occur.

Overvoltage Protection

Another situation where it is desirable to use an integrator occurs in the protection against overvoltage in high-side switches (Simas, Buxo - 1989).

It has been shown that when a CMOS inverter is driven into dynamic switching on a capacitive load, the maximum current value through the inverter is a function of the input voltage slope. Thus, a current value may be defined as a reference for the control circuit of the power device to be "smartly" protected (fig. 10). This technique also provides a high performance dv/dt detection, for the efficient drive of power devices.

An overvoltage protection for low-side switches which makes use of an analog feedback loop has also been presented (Simas, Piedade - 1987). This technique allows the control of the transient overvoltage in a predictable way, with high precision, independently of the power supply voltage and of the load, by acting upon the drain current through the gate drive circuit.

This feature has already been implemented in some power transistors. In fact, design modifications have ensured that the voltage drop on the source-substrate region for all operating conditions remains below the threshold voltage of the parasitic bipolar transistor (Reinmuth, Lorenz - 1989).

Battery Discharge Detector

Figure 11 shows a battery discharge detector circuit. This circuit usually has the M1 transistor operating in saturation with $V_A > V_{DD} + |V_{th}|$, where V_{th} is its

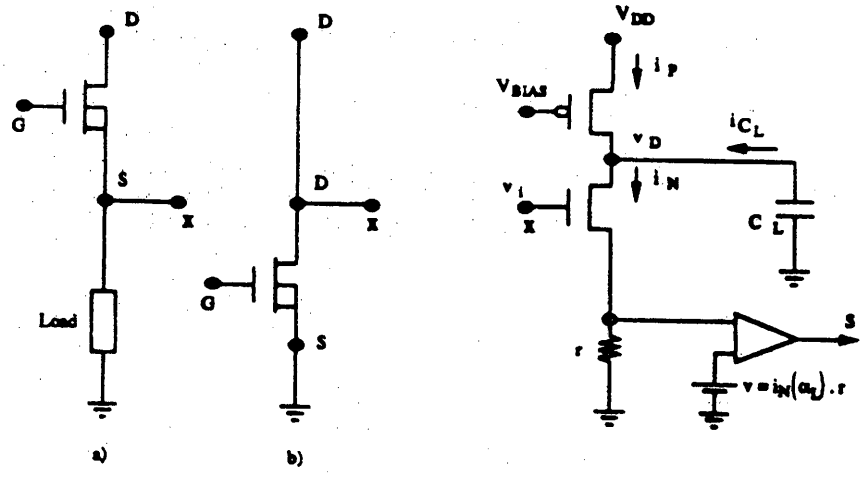

Figura 10. A dv/dt detection circuit.

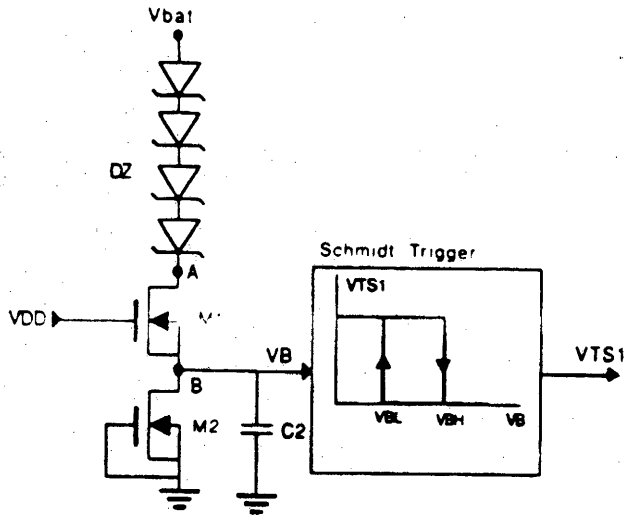

Figura 11. Battery discharge detection circuit

threshold voltage. Thus, its drain current doesn't depend on the drain voltage, and M2 drain voltage is not affected by the battery voltage and M2 operates in the saturation region.

When $V_A < V_{DD} + | V_{th} |$, M1 is in the triode region, and its drain current is no longer constant. Thus M2 drain voltage decreases and the Schmidt trigger goes high. This command signal turns the VDMOS off through the charge pump circuit.

All these functions call for adequate and low cost technological solutions. Well established low cost CMOS technologies are also being used to attempt the implementation of smart power devices (Behrens - 1989).

5. CAD TOOLS

To overcome Smart Power design problems, or to optimize the design of new power processing topologies that use power semiconductor devices operating with ever increasing switching frequencies, it is extremely important to have a good characterization of the power MOS transistor using a simple model, because the transient analysis should be obtained with reasonable computing time. With Smart Power devices we have simultaneously the demanding transients of the power circuits topologies and the large number of devices of the control

The accurate characterization of MOSFET internal capacitances is of fundamental importance both in the design of Smart Power devices and of the new high fre-

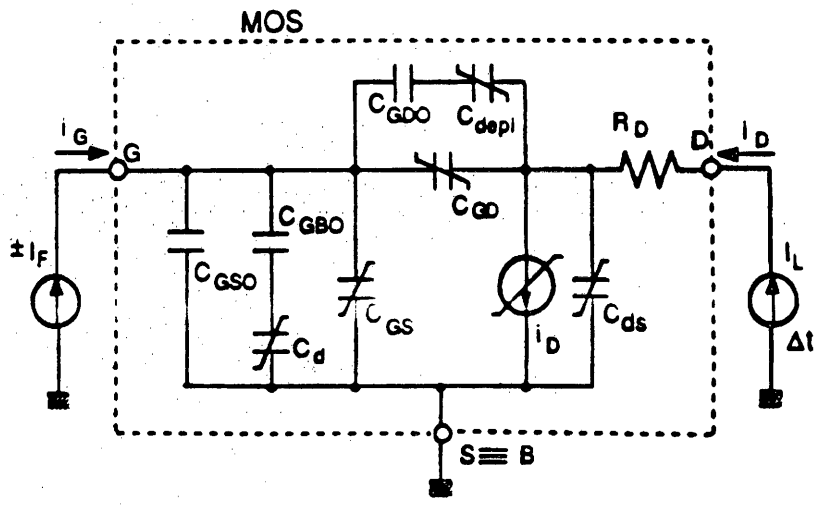

Figura 12. VDMOS equivalent model circuit under gate and drain constant currents.

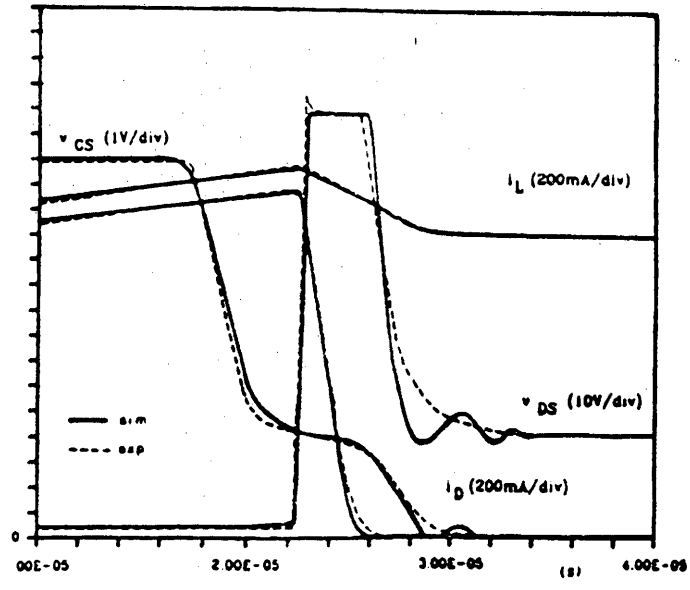

Figura 13. SPICE simulation results of the turn-off of an overvoltage protected VDMOS.

quency resonant, quasi-resonant, semi-resonant and PWM-quasi-resonant power converters, because these capacitances determine the timing and the tuning of the circuit.

A power VDMOS transistor model, with special emphasis on the internal capacitances was presented elsewhere by the author (Simas et als - Vol.4, nº 3 - 1989). The modelling technique is based on device operation under gate and drain constant current conditions. These conditions permit to enhance capacitive effects, reducing the series resistive effects, and have been suggested by a previous study of transistor physical behavior in the different regions of operation (off, triode and saturation) (Simas et als - 1987). The MOS capacitances are modelled by piecewise equations (fig 12).

The method leads to a simplifield model, the parameters of which are easily obtained by external measurements only. The model is easily implemented in the SPICE family of programs, either directly or not depending on the version available.

By making use of the previously referred model, it is possible to analyze smart power devices behavior (Simas et als - 1989) as well as switching power electronic converters, either using resonant configurations or not, with accuracy. The performance of a PWM converter using the overvoltage protection feedback technique referred previously, namely its stability was analysed by simulation. Fig. 13 shows the simulation results, using the SPICE program, of the protected VDMOS turn-off behavior

compared with experimental results. This accurate modelling, has also been proved useful as a computer aided design tool for the analysis and optimization of quasi-resonant converters (Simas et als - vol. 4, nº 3 - 1989).

6. CONCLUSIONS

This paper presents a brief review of the ability of MOS technologies, to combine smart function circuits with the power MOS device in the same chip. Expected trends have been discussed and some special functions have been referred and summarily described. Limitations still not overcome have been outline. The extreme importance of the accurate modelling of the power device by a simple model have been stressed. Such an accurate model is a very useful tool for the design of either smart power devices or switching converters.

It is to be desired that tremendous technology development in recent years will encourage Industry, Government Agencies, and Universities to cooperate in exploring all the exciting new possibilities that have been created, and soon it will be possible to gain enormous advantages in productivity and efficiency improvements.

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